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Service Hand Book

Panasonic
AUTO PRODUCTS
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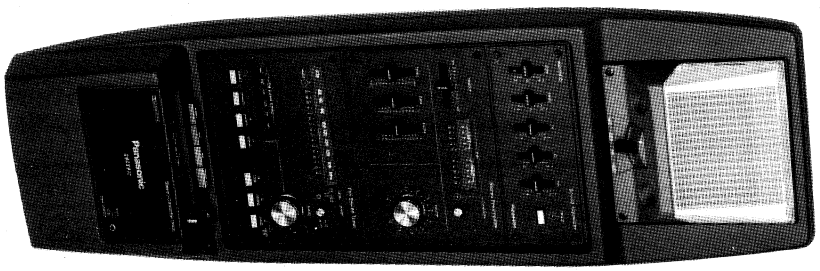
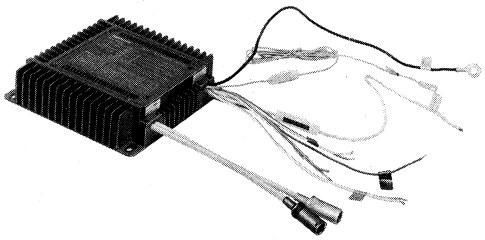
COCKPIT

Car Audio

RM-610/RM-E610

Overhead Console Type Hi-Fi Car Audio System





General

Power Source:	DC 13.8 V (11–16 V usable) Negative ground only
Power Consumption:	12.5A at rated power output
Dimensions:	Console unit; 27-3/4"(L)×9-1/16"(W)×1-1/2"(D) (Cassette Deck Section Depth 3") Power amplifier; 8-1/16"(W)×8-1/8"(D)×2"(H)
Weight:	Console unit; 8 lb 3 oz Power amplifier; 5 lb 1 oz

FM Tuner Section

Frequency Range:	88–108 MHz
Usable Sensitivity:	16 dBf (1.7μV/75Ω, S/N 30 dB, IHF '75)
50 dB Quieting Sensitivity:	18 dBf (2.2μV/75Ω)
Signal to Noise Ratio:	65 dB
Image Rejection:	65 dB
IF Rejection:	95 dB
RF IMD Rejectin:	80 dB
Frequency Response:	20–15,000 Hz
Stereo Separation:	40 dB at 1,000 Hz

Preamplifier Section

Tone Control:	Bass 100 Hz ±10 dB Treble 10 kHz ±10 dB Loudness 100 Hz ±8 dB

Cassette Deck Section

Wow and Flutter:	0.2% (WRMS)
Cross-Talk:	57 dB
Signal to Noise Ratio:	60 dB Dolby NR in 52 dB Dolby NR out
Frequency Response:	30–14,000 Hz
Stereo Separation:	40 dB at 1,000 Hz

Power Amplifier

Rated Power Output:	Total 60 watts sine wave RMS power into 4 ohms, all channel driven, from 20–20,000 Hz, 0.5% total harmonic distortion Front; 10 watts per channel Rear; 20 watts per channel
Max. Power Output:	Total 120 watts RMS Front; 20 watts per channel Rear; 40 watts per channel
Distortion:	0.07% at ±3 dB at Rated Power 1,000 Hz
Frequency Response:	20–40,000 Hz ±3 dB at 1 Watt
Signal to Noise Ratio:	82 dB

Specifications are subject to change without notice.

Panasonic®

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5770 Ambler Drive, Mississauga,
Ontario, L4W 2T3

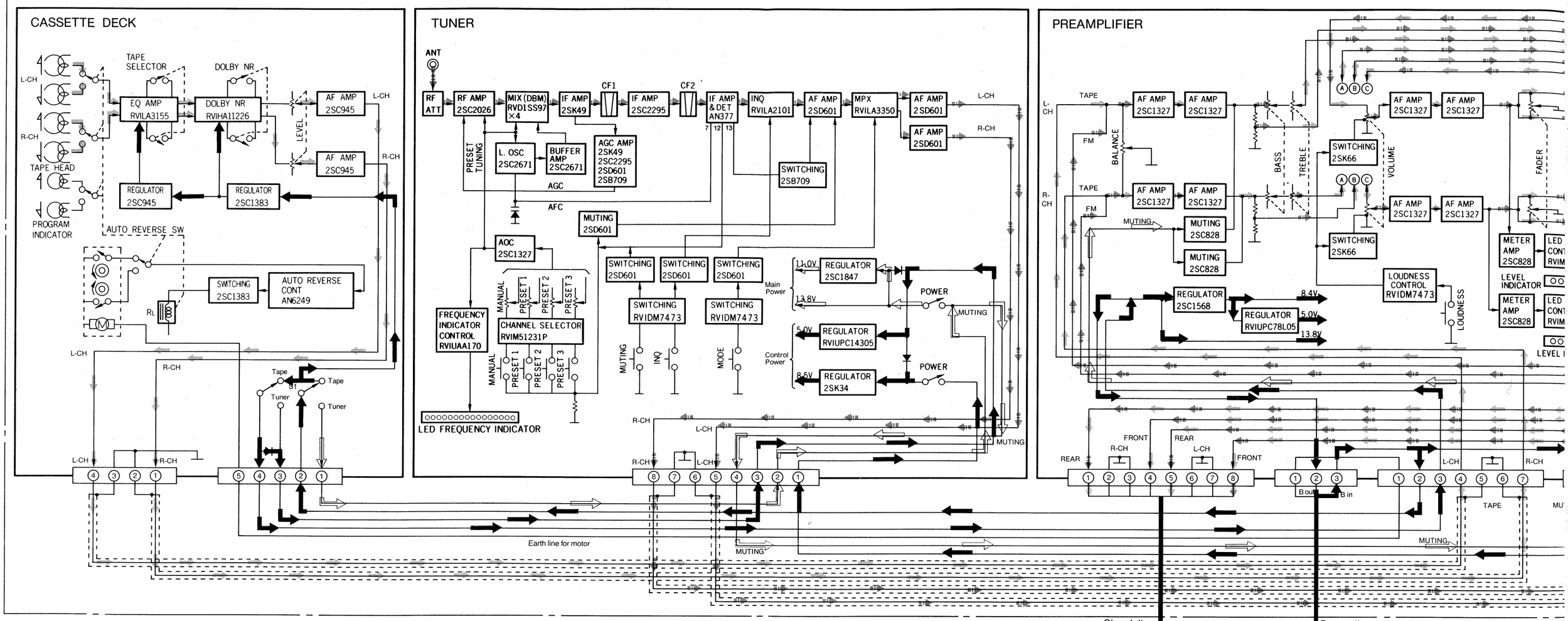
Contents

1. Introduction

Is it possible to introduce high fidelity sound into a moving automobile, that is subject to road noise, ignition noise and other types of interference, as well as varying FM signal conditions, with good results? Fortunately, the answer is yes, but it ins't simple. To enjoy high fidelity audio in a moving vehicle, certain special performance and functional criteria must be met; special circuits to reduce noise and improve reception under adverse conditions, as well as rugged construction to resist vibration and the thumps and bumps of the road. The research and development of a product to meet these requirements gave birth to the RM-610. The RM-610 is capable of achieving excellent high fidelity performance, while the car is standing still, or on the move, and in both weak and strong FM signal areas.

The RM-610 is made up of a number of discrete Hi-Fi type components. The cassette deck features a Dolby Noise Reduction (NR) system. A high-power main amplifier provides audio power to spare, and at very respectably low distortion. The graphic equalizer is optional equipment in the RM-610. The equalizer makes it possible to adjust the frequency response of the system, to make up for differences in personal listening habits, and for variations found in different accoustical environments. For maximum flexibility, speakers are not included in the RM-610. There is a wide selection of good quality speakers for car use; that come in a variety of shapes and sizes, and in different types of enclosures. Thus it is possible to optimumly select speakers that are most likely to fit in the car, and please the listener.

2. Block Diagram



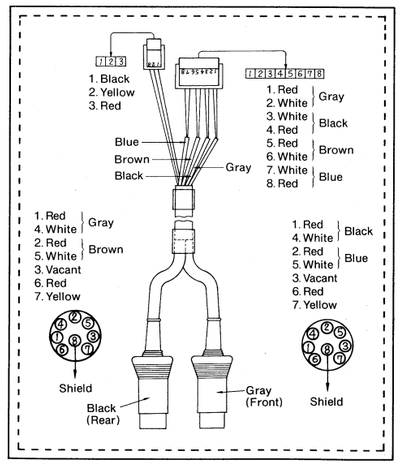
Notes:

Tape signal line.....

FM signal line.....

Power Supply line.....

Power supply line when tuner used...



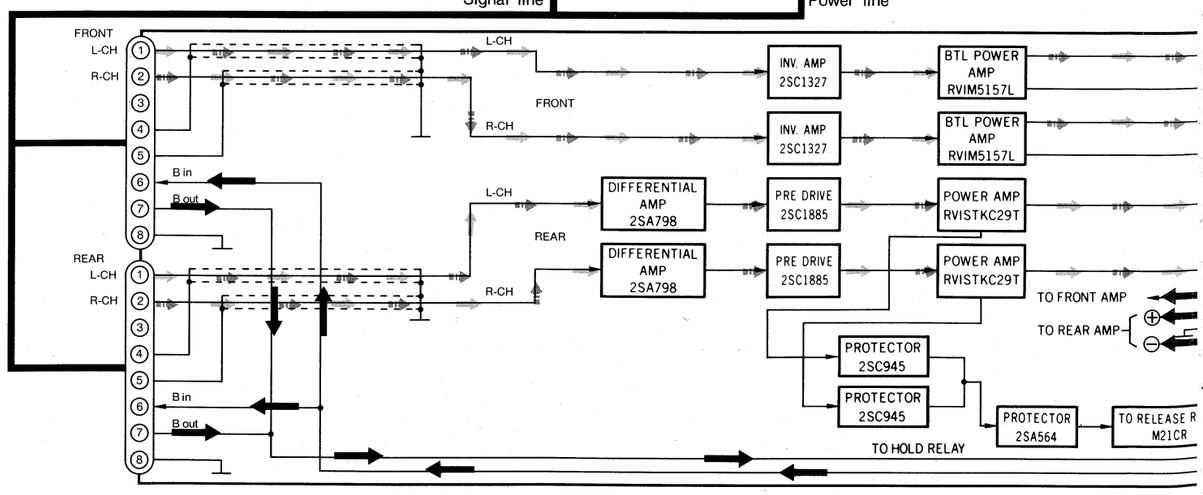
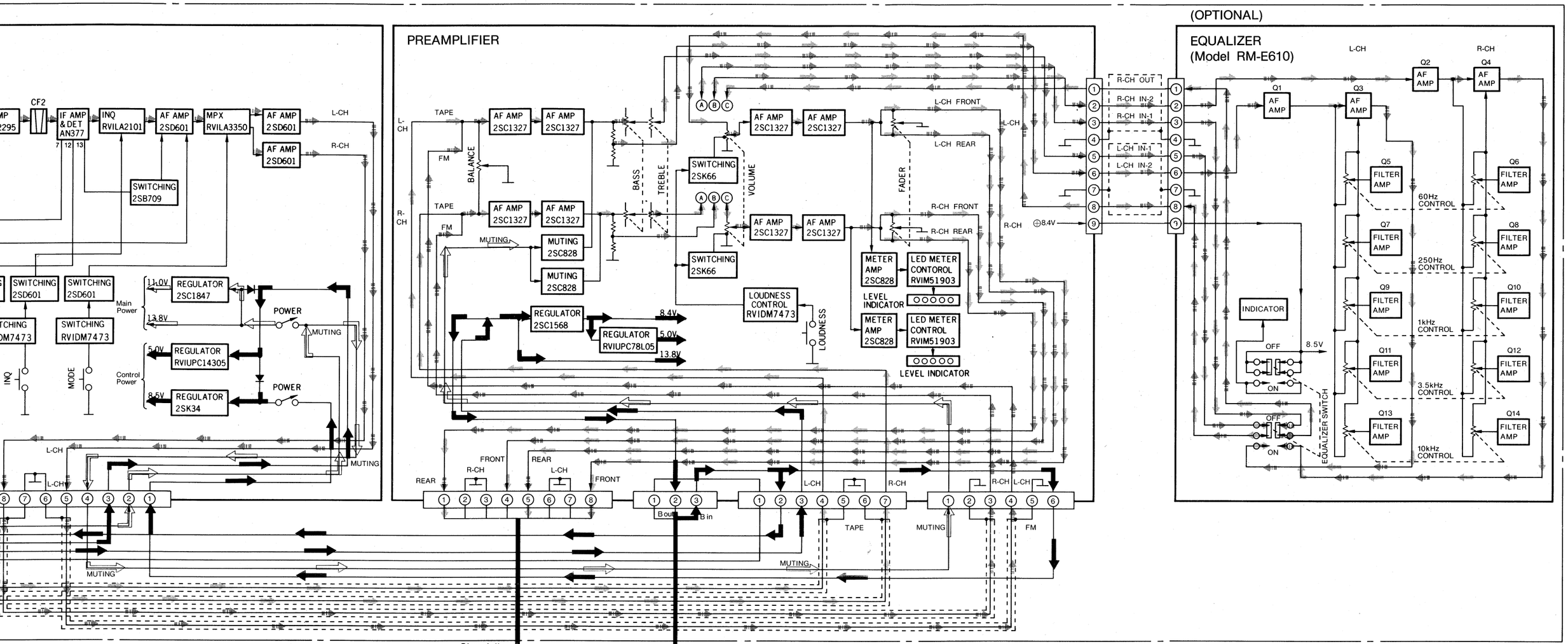
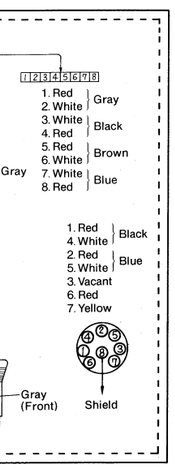


Fig. 1

2. Block Diagram





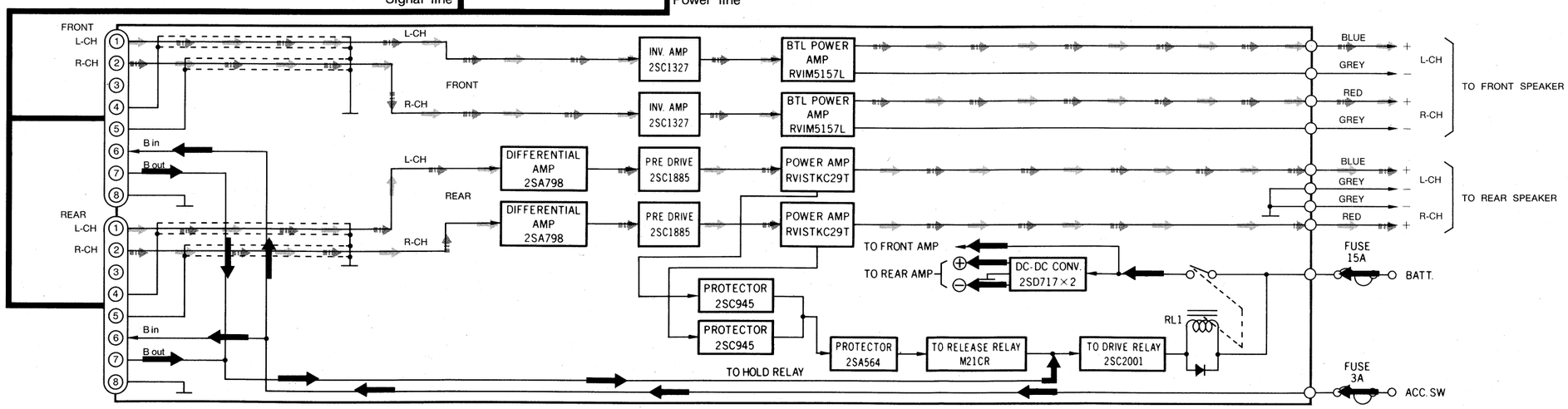


Fig. 1

Circuit Description

3. Tuning Circuit

The FM tuner takes advantage of an electronic tuning system employing varactors (voltage controlled variable capacitance diodes). There are no variable capacitors or variable inductors to be manually turned to tune in a radio station, as there are in conventional radio tuners.

Tuning is accomplished electronically by changing the voltage across varactors D3 to D6. See Fig. 2. As the voltage changes, so does the varactors capacitance and tunes the RF amplifier's (Q1) input and output circuits, local oscillator (Q2), and mixer (D7 to D10). The voltage across these varactors is controlled by variable resistors (VR101 to VR104). These resistros are switched into the circuit one at a time, when their related switches (S1 to S4) are pressed. Switch S1 and VR101 operate the manual tuning function, and switches S2 to S4 along with there related variable resistors VR102 to VR104 operate the preset stations. Tuning is as simple as turning a volume control. Here's how it works:

(A) Press S3

Input 3 is grounded through R104, output 3 goes low and allows current to flow through LED D111 and VR103. See Fig. 2. The LED lights up, and the voltage drop across VR103 is applied to the base of Q101 through D103. The amount of voltage on the base of Q101 depends upon the setting of VR103. The higher the applied voltage to the base, the more Q101 conducts, the greater the voltage developed across the voltage divider made up of Q101, R142, R143 and R144, and the greater the voltage applied to the varactors. The converse is also true, if a lower voltage is applied to the base of Q101, a lower voltage will be applied to the varactors.

(B) Press S2

Input 2 is grounded through R104, output 2 goes low and output 3 is returned to high. The same action occurs as when S3 was pressed, except that now LED D110 is on, and VR102 determines how much Q101 will conduct and develop a control voltage to go to the varactors. And so it goes when any of the other selector switches are pressed.

It is possible to tune the entire FM broadcast band on any of the 3 preset positions, as well as the manual position. If the manual position is set to a station, as well as the preset positions, then it is possible to select any one of 4 stations at the push of a button, without any further tuning.

Preset tuning selector 1 priority (S2)

Preset your most popular station on Preset Tuning Selector 1. This station will then be heard first when the power switch is turned on. It is necessary to instruct IC101 to turn on one of the stations after each time the power has been shut off.

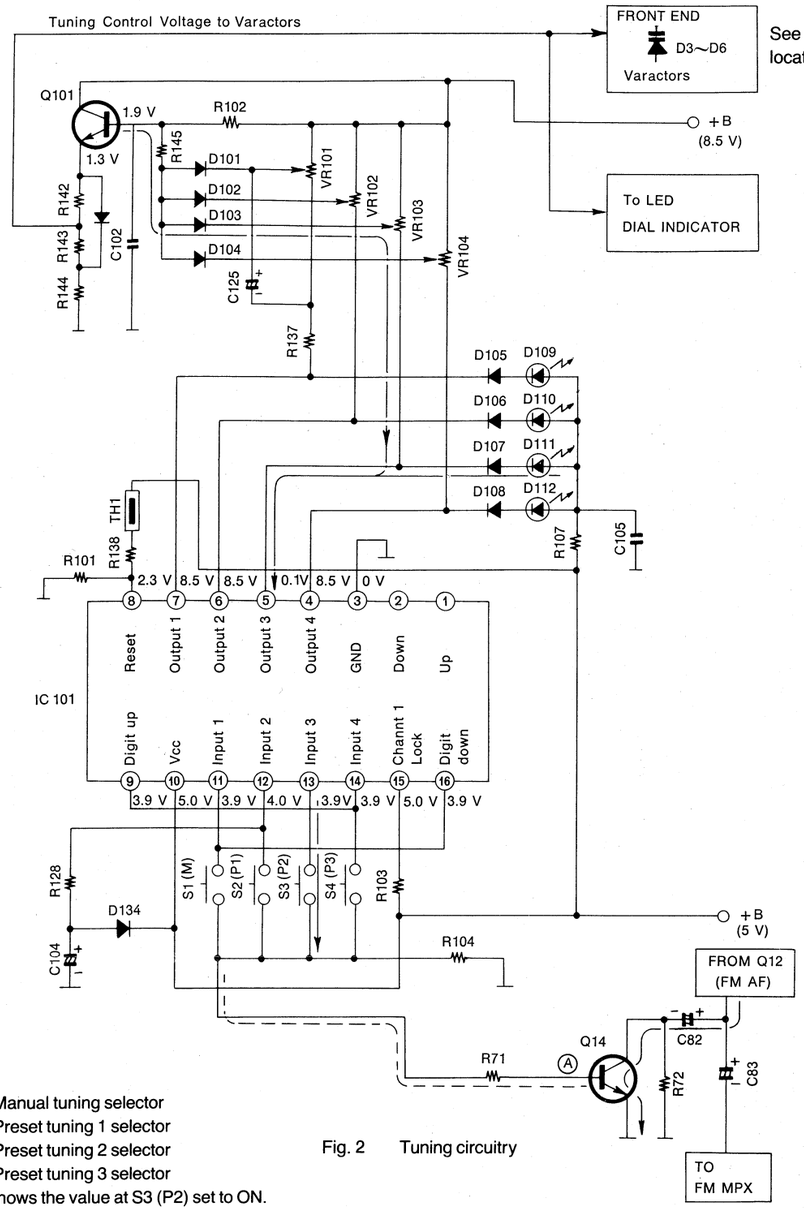
This is done automatically, as follows: current flows through C104 and R128, when the power is first turned on and it essentially does the same work as pressing S2 manually. When C104 charges up to the B+level, it is effectively out of the circuit, and allows S1 to S4 to function when pressed, at any time.

Tuning circuit functions

Switch Position Pushed	IC101 Terminal (Low)	LED Illuminated	VR in control
S1 (Manual)	⑦	D109	VR101
S2 (Preset 1)	⑥	D110	VR102
S3 (Preset 2)	⑤	D111	VR103
S4 (Preset 3)	④	D112	VR104

Muting

When any one of switches S1 to S4 is pressed to change stations, or to momentarily cut the radio station audio signal, Q14 is turned on and provides a low impedance path from the audio amplifier Q12 to ground. Releasing the switch turns Q14 off and allows the radio program to be heard.



NOTE: S1 ..... Manual tuning selector
S2 ..... Preset tuning 1 selector
S3 ..... Preset tuning 2 selector
S4 ..... Preset tuning 3 selector
DC voltage shows the value at S3 (P2) set to ON.

Fig. 2 Tuning circuitry

ANT & RF AMP Frequency D3/D5/D6	Local OSC Frequency D4	Control Voltage DC Volts (Approx.)
88.1 MHz	98.8 MHz	1.18 V
90.1 MHz	100.8 MHz	1.45 V
94.1 MHz	104.8 MHz	2.06 V
98.1 MHz	108.8 MHz	2.86 V
102.1 MHz	112.8 MHz	3.92 V
106.1 MHz	116.8 MHz	5.33 V
107.9 MHz	118.7 MHz	6.12 V

Table 1. Control Voltage required to tune the VCO for FM Stations

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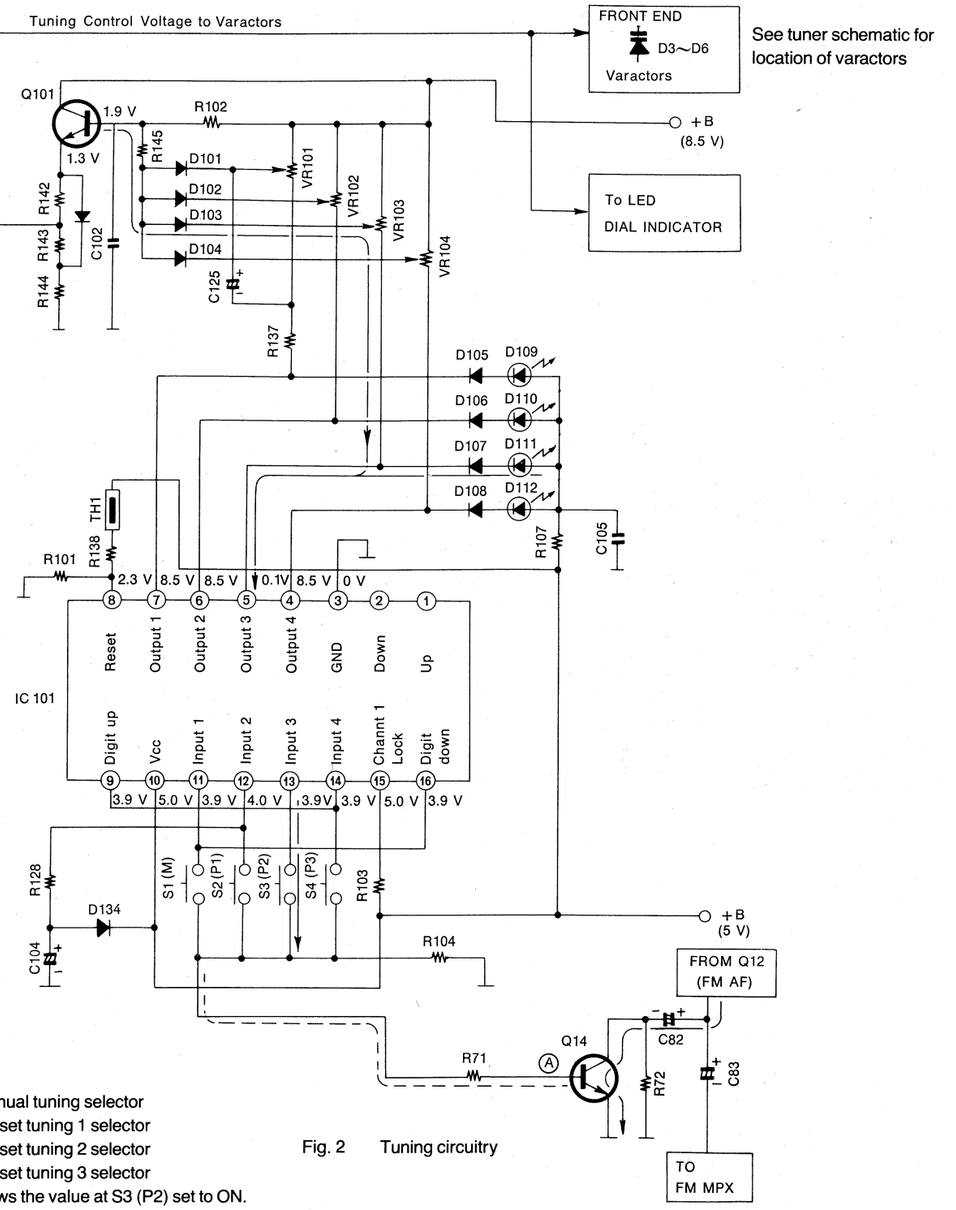

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Table 1. Control Voltage required to tune the VCO for FM Stations

4. Tuning Dial Indicator

The LED-indication tuning dial circuitry illuminates the applicable LED's (D114 to D129) according to the tuned frequency. IC103 is used to drive the LED's. The tuning voltage applied to the variable-capacitance diodes is the IC's voltage control input, pin ⑪. The order of illumination of the LED's changes according to the change in this voltage. See Table. 2.

As the tuning frequency goes higher, the illuminated LED's changes in the order D129-D114.

- Terminals ⑭ and ⑯ determines LED brightness.
- Terminal ⑮ determines the range of LED brightness.
- Terminal ⑪ is for control voltage from the tuning circutry. Each LED is driven according to this input voltage.
- The potential difference between terminals ⑫ and ⑬ corresponds to the range of LED indication voltage variation of terminal ⑪ voltage.

The maximum value of LED indication voltage is determined by the voltage applied to terminal ⑬, and the minimum value is determined by the voltage applied to terminal ⑫.

When the LED indication voltage is less than the lower limit, the first LED (D129) remains illuminated, if more than the upper limit, the last LED (D114) remains illuminated.

- Terminal ⑩ is for power supply, and terminal ① is for grounding.
- The eight terminals ⑥ — ⑨ and ② — ⑤ are output terminals for LED control.
  Terminals ⑥ — ⑨ are connected to the anode side of each LED, and become high level when the output is ON.
  Terminals ② — ⑤ are connected to the cathode side of each LED, and become low level when the output is ON.
- Table 2 shows the relationship between each output terminal and LED illumination position according to changes in the voltage applied to terminal ⑪.

Frequency (MHz)		88															108
LED illumination		D129	D128	D127	D126	D125	D124	D123	D122	D121	D120	D119	D118	D117	D116	D115	D114
Voltage change at terminal ⑪, IC103		0.2V (Min.) ◄															2.2V (Max.) ►
Terminal No. of IC103	②	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L
	③	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	H
	④	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H
	⑤	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H	H
	⑥	L	L	L	H	H	L	L	L	L	L	L	H	H	L	L	L
	⑦	L	L	H	L	L	H	L	L	L	L	H	L	L	H	L	L
	⑧	L	H	L	L	L	L	H	L	L	H	L	L	L	L	H	L
	⑨	H	L	L	L	L	L	L	H	H	L	L	L	L	L	L	H

Note: For 0.2 V, D129 Lights up . . . ④ Low Level (L) & ⑨ High Level (H).

Table-2 Output terminals and LED illumination vs. Voltage change of terminal ⑪, IC103

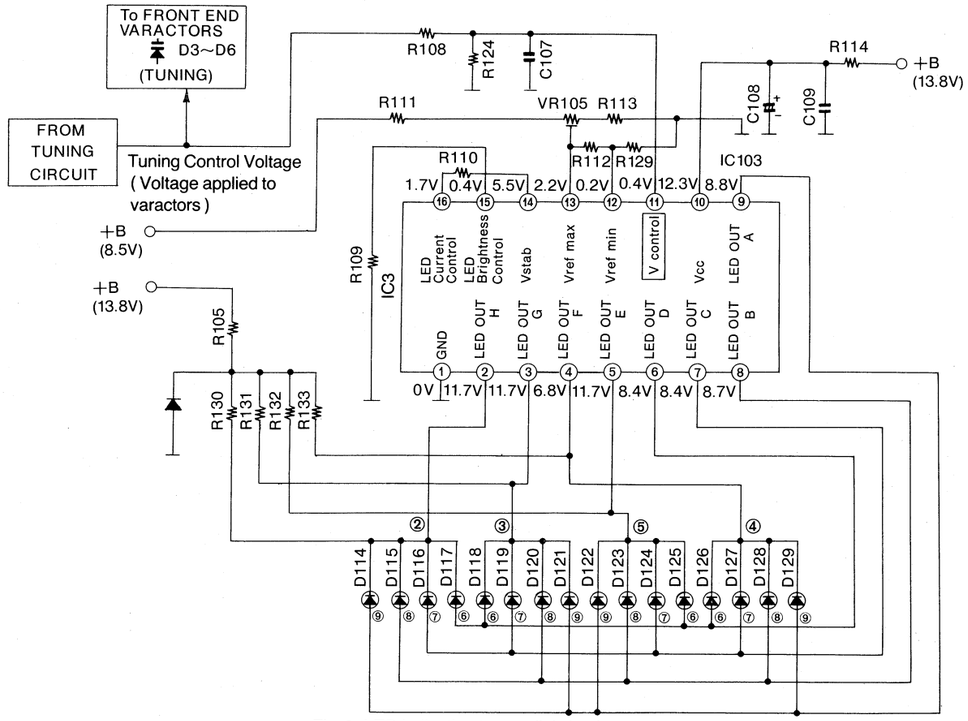


Fig. 3. LED indication tuning dial circuitry

5. Mixer Circuit

Double-balanced mixer is used in order to provide good frequency characteristics with wide dynamic range, which minimizes unnecessary signals in the output side.
RF input signal (fi) is applied to Terminal ⑥ of Ⓛ6 and diodes D_7–D_{10}.
The local oscillator signal is applied to terminal ② of Ⓛ7. After passing through Ⓛ7, frequency conversion takes place at diodes D_7–D_{10}.
The sum and difference signals of fi & fL and their harmonics appear during frequency conversion.

Because balance circuits, consisting Ⓛ6 & Ⓛ7, are employed, signals other than fi+fL and fi−fL are cancelled each other and only fi+fL & fi−fL signals appear at terminal 6 of Ⓛ7 as an output.
Because the necessary IF output signal is only fi−fL, it is taken out after passing through filter (T_2 & C_{32}), and applied to IF Amp.
Impedance of R_{26} & C_{33} is high to the IF signal.
Signals higher than input signal (fi) and local oscillator signal (fL) are terminated by 50 Ω.

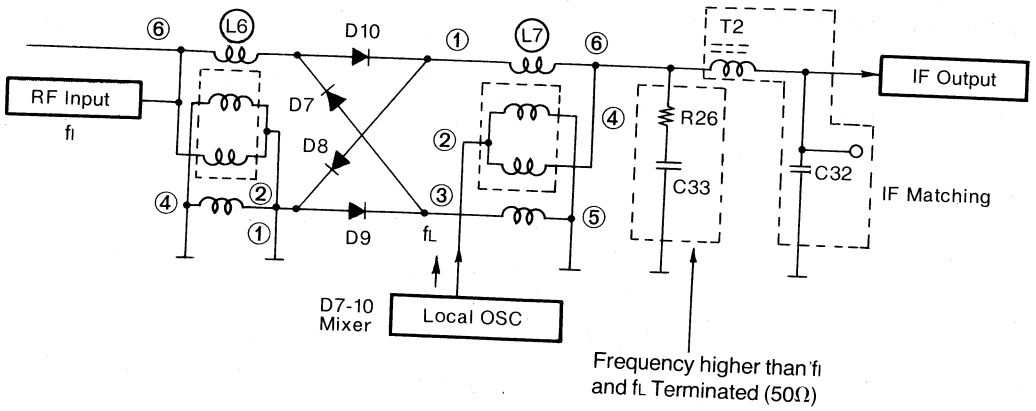


Fig. 4 Mixer Circuit

6. AGC (Automatic Gain Control) Circuit

Transistors Q6 to Q9 applies a varying voltage (according to signal strength) to switching diodes D2 and D18 in the antenna tuning circuit to vary the Q for a 35~40 dB range of signal strength. A buffer amplifier, with wide dynamic range, couples the AGC circuit to the IF.

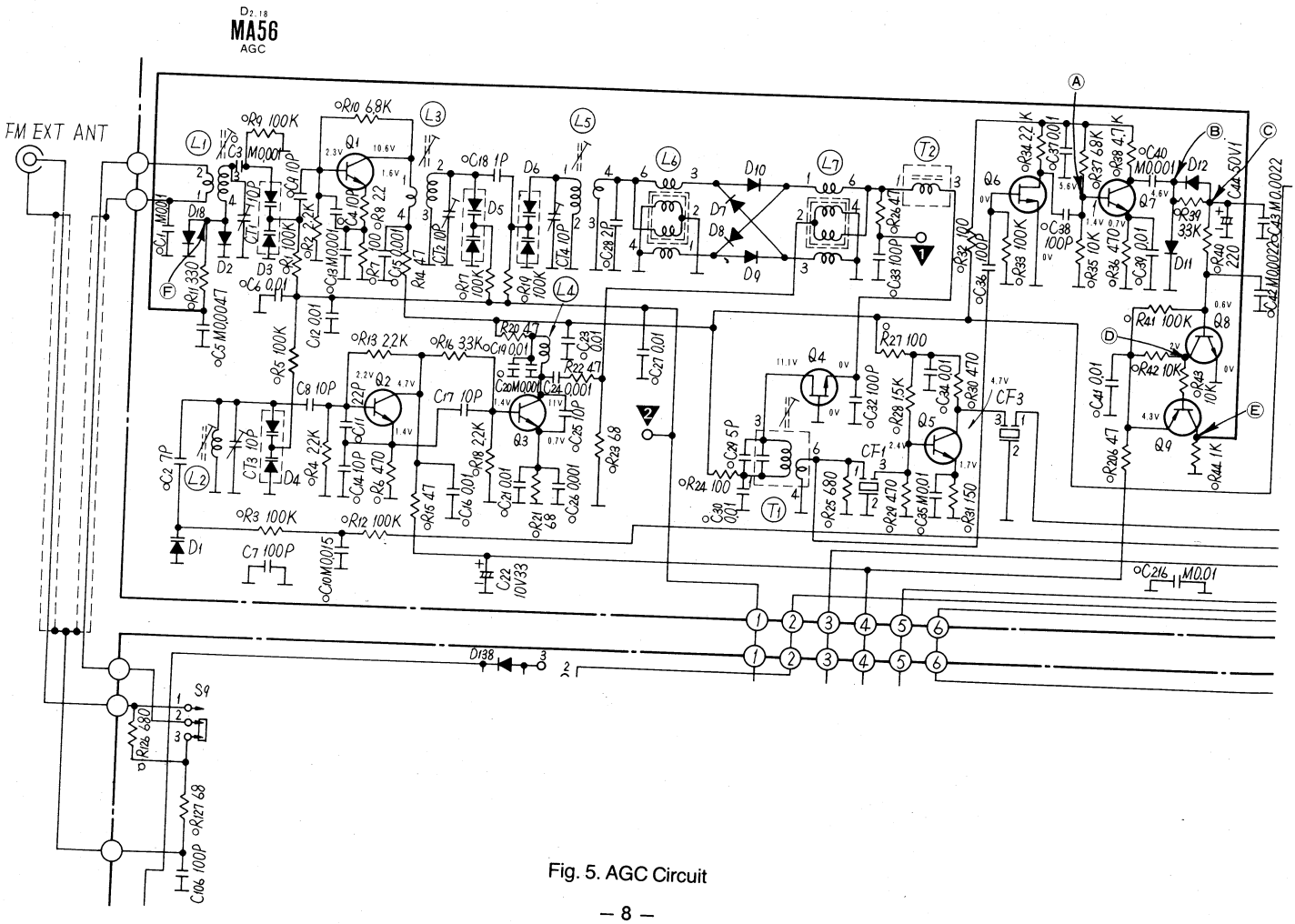


Fig. 5. AGC Circuit

AGC amplifier operation during high signal strength input (Refer to figure 5.)

1. When a strong signal is received from the antenna, it the signal is amplified by the buffer amplifier Q6, and passed on to the base of Q7 [point Ⓐ].

2. Because only the amplified IF signal appearing at point Ⓑ, is rectified at D11 and D12, and smoothed at C44, the potential at point Ⓒ reduces in proportion to the signal strength.

3. As a result, current flow at point Ⓓ becomes low, and potential increases.

4. When potential at point Ⓓ increases, current flow between the collector and emitter become difficult, and consequently, potential at point Ⓔ decreases.

5. Because potential decreases at point Ⓔ, the voltage at point Ⓕ decreases in the same way, and switching diodes D2 and D18 change from ON to OFF. The condition of the antenna tuning circuitry is thereby such that resistance is directly connected to the secondary coil, and, as a result, the Q is damped.

6. Consequently, the Q of this resonance circuitry decreases, and RF gain lowers.

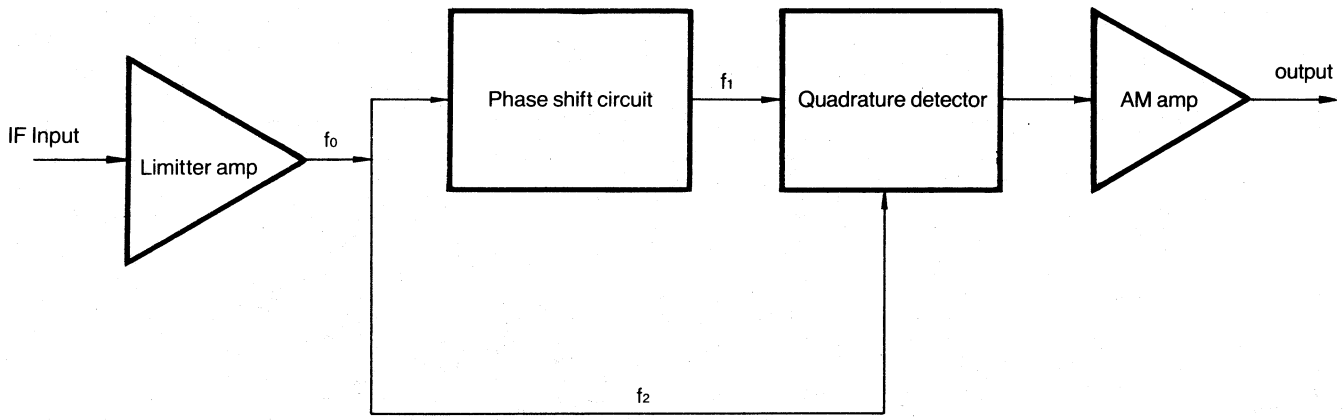
7. FM Detector Circuit

The RM-610 uses a quadrature detector to detect the FM signal.

Basic Operation

The quadrature detector, 3 IF limiter amplifiers and an AM amplifier are all located on a single AN377 chip (IC 1). The quadrature phase shift circuit (essentially made up of inductance, capacitance and resistance) is externally mounted.

The IF signal is fed into the 1st IF limiter amplifier, and fed through to the phase shift circuit and the quadrature detector. By the time the signal passes through the 3 stages of limiting the tops and bottoms of the IF signals waveform are clipped, and what was a series of sinewaves now looks like squarewaves. The frequency of the IF signal varies above and below the 10.7 MHz IF center frequency, in step with the audio signal. The quadrature phase shift circuit follows the frequency shifts of the IF signal and produces a sinewave signal of the same order of frequencies, accept that as the frequency changes the phase difference between the two signals changes to more or less than 90 degrees, as follows.



When the IF signal is 10.7 MHz (the center frequency), as would be the case if no modulation is present, the signal from the phase shift circuit will be 90° out of phase; the average value of the output signal will be zero. See Fig. 7, Figs. 8 and 9 show what happens when the IF signal is above and below the IF center frequency. The resultant output signal becomes positive or negative, respectively. Relative waveforms in the quadrature detector are as follws:

(a) The IF signal equals 10.7 MHz, the phase shift signal is 90° out of phase, and the output signal is essentially zero.

Quadrature Phase Shift Signal

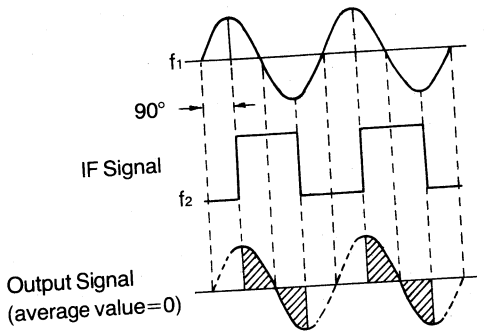


Fig. 7

(b) The IF signal is less than 10.7 MHz, phase shift signal is less than 90° of phase, and the output signal is essentially positive.

Quadrature Phase Shift Signal

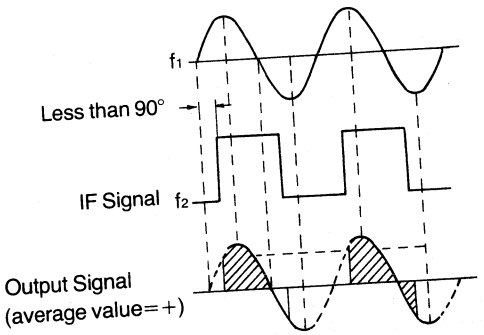


Fig. 8

(c) The IF signal is greater than 10.7 MHz, the phase shift signal is greater than 90° out of phase, and the output signal is essentially negative.

Quadrature Phase Shift Signal

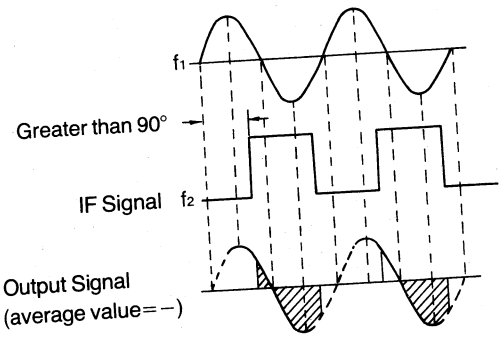


Fig. 9

The resultant output signal is derived in the quadrature detector by comparing the IF signal and the phase shift signal. The quadrature detector is actually a balanced differential amplifier (See Fig. 10) which is impervious to thermal variations and provides an undistorted audio signal to the AM amplifier.

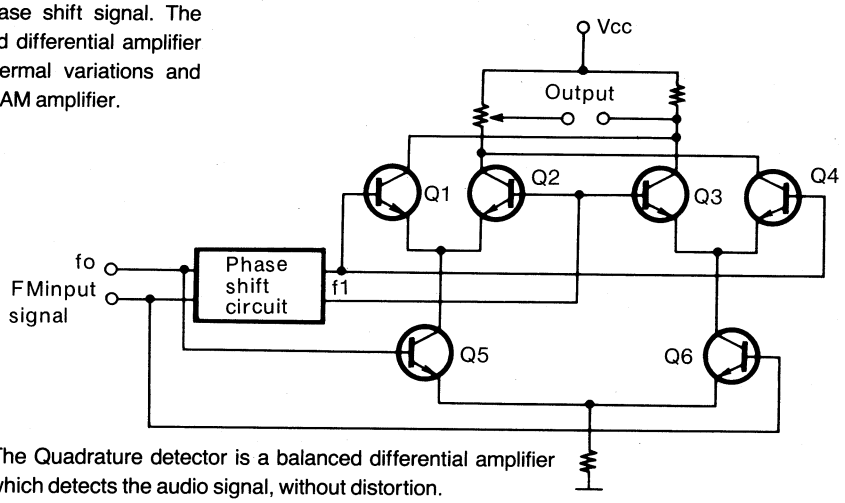


Fig. 10. The Quadrature detector is a balanced differential amplifier which detects the audio signal, without distortion.

8. MPX Crcuit

Mode control circuit (Stereo Auto/Mono Switch)

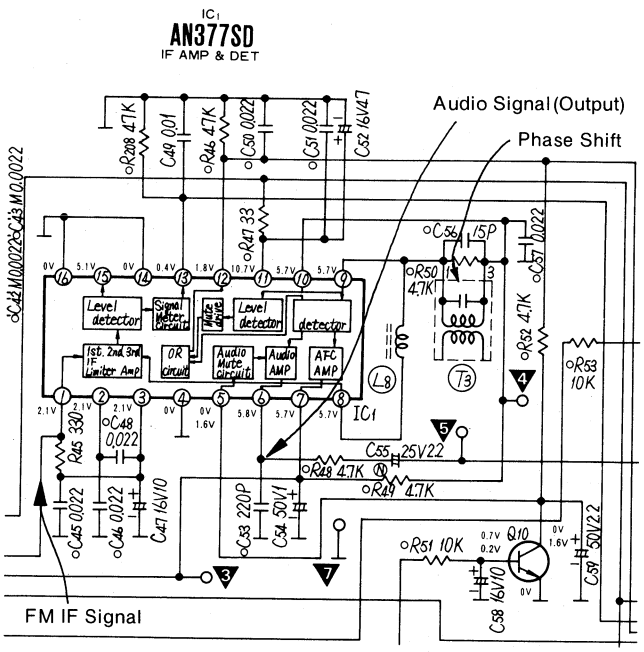


Fig. 11 FM Detector Circuit-RM-610

When the mode switch (S5) is pressed, the mode is FM auto, (LED lights up). A stereo program will be automatically received in stereo, and, if the program is a mono broadcast, it will automatically be received in mono.
When the mode switch (S5) is pressed once, the mode reverses to the mono. In this case, a stereo program will be heard in mono and the LED does not light up.

1. When the mode switch (S5) is pressed, DC output Level (Q) of the J-K flip-flop (IC104) becomes Low, and switching transistor Q15 is in the OFF condition. At this time, the mode LED (D131) illuminates.
2. Because Q15 is OFF, the MPX IC (IC3) is not affected, and performs ordinary operation. In other words, at this time the mode is in the FM auto condition.
3. When in the FM auto mode, and (S5) is pressed once, DC output Level (Q) changes from Low to High level, and Q15 switches ON.
4. When Q15 switches ON, the electric potential of point Ⓐ in figure 12 drops, and the FM reception signal is forced to become monaural (Refer to the operation explanation of the PLL FM decoder.), finally making the mode become monaural.
5. In this way, pushing the mode switch (S5) reverses the mode.

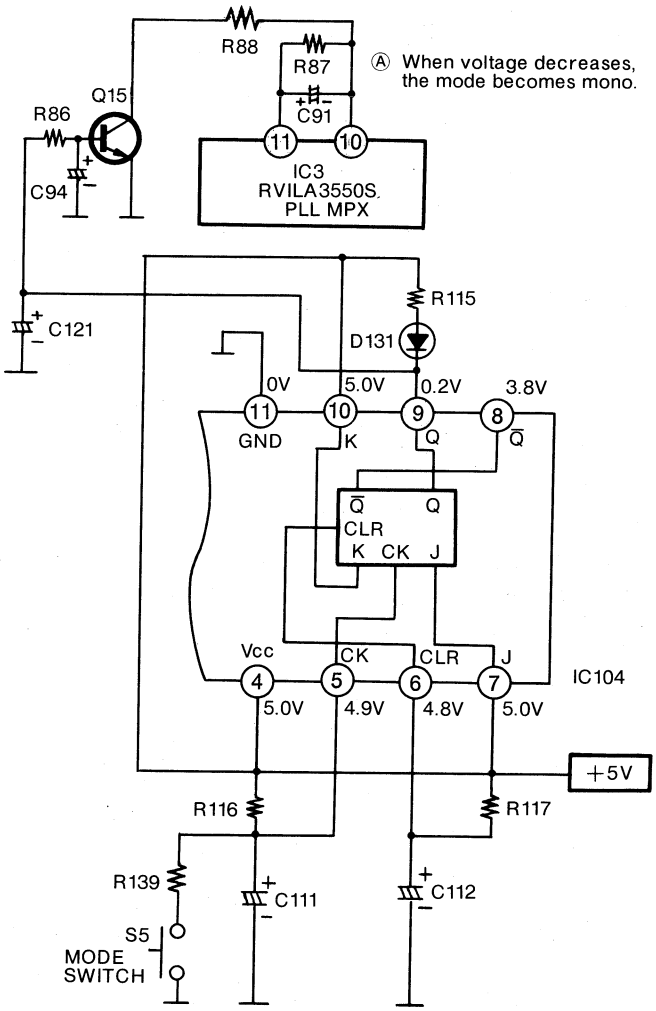


Fig. 12 Mode control circuit

Automatic Stereo/Mono Switching

When the input signal drops to about 35 dB, or less, the control voltage from IC1, IF stage, terminal ⑬ decreases and lowers the voltage on IC3, PLL MPX, stereo/mono switching terminal ⑩. This disables the PLL MPX and results in mono operation.

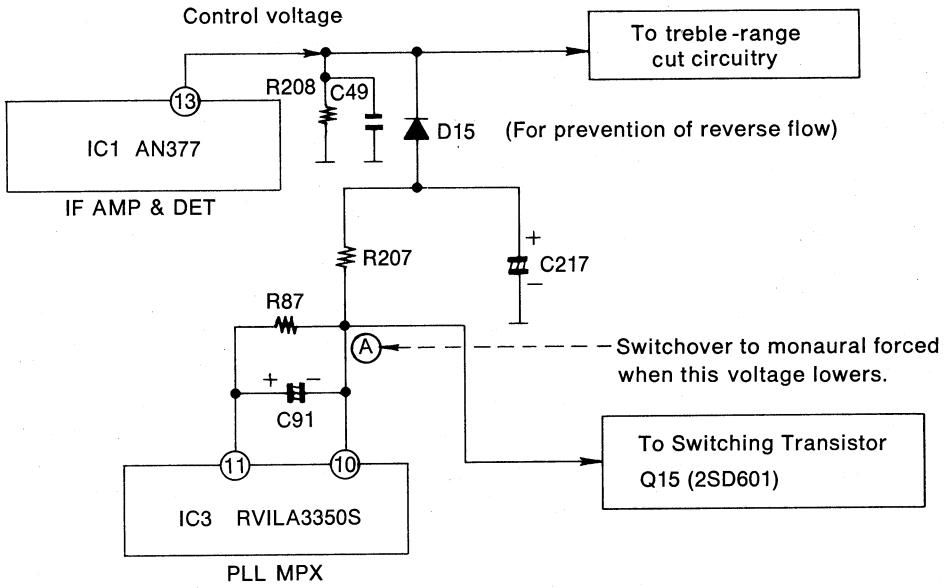


Fig. 13 Automatic stereo/mono switching circuitry

FM stereo signal input level	IC pin ⑬ voltage	Point Ⓐ voltage	MODE
Approx. 35 dB or more	HIGH	HIGH	STEREO
Approx. 35 dB or less	LOW	LOW	MONO

If there are rapid changes in field strength near 35 dB, there could be rapid changes from stereo-to-mono-to-stereo operation, and cause an undesirerable sound effect. To prevent this type of rapid switching action, a delay component (C217) has been added. The time constant is fast when the signal becomes weak, and slow when the signal becomes strong. Thus the mono or stereo mode will stay on longer to take better advantage of the weak fluxuating signal.

Phase Locked Loop (PLL) FM Stereo Decoder System

A. Advantages

Both matrix and switching type systems generate a 38-kHz local signal in the receiver to "reconstruct" the 38-kHz suppressed subcarrier in the transmitted stereo signal. Any discrepancies in the proper phase or frequency relationship between the stereo signal's subcarrier and the 38-kHz local signal can cause the separation of the right and left channels to deteriorate, and other forms of distortion.

To prevent these discrepancies, the oscillator and frequency controlling circuits must be carefully designed, and parts must be carefully selected. Even changes caused by temperature and aging can cause serious problems. To eliminate or at least minimize these problems, a PLL system is used to provide accurate frequency and phase relationships within the receiver.

B. Major Components

A PLL circuit is like an electronic servo system designed to self-correct and provide an extremely accurate output. It is typically composed of a Phase Comparator (PC), Low-Pass Filter (LPF), and a Voltage Controlled Oscillator (VCO). See Fig. 14.

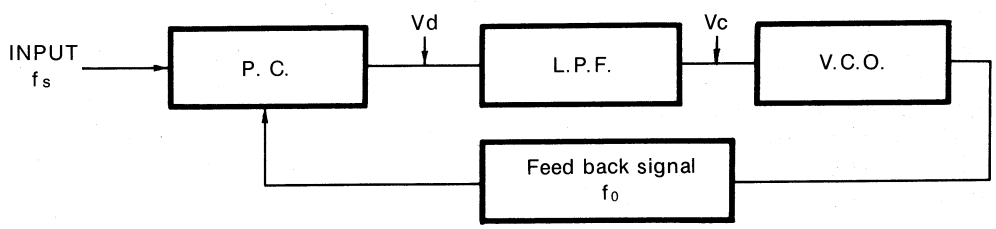


Fig. 14. Basic PLL

Typical PLL circuit is essentially a closed loop. The feedback signal (f_o) is compared with the standard input signal (f_s). Differences in these two signals (f_s & f_o), if any, produce an error correcting voltage (V_d) to keep the VCO frequency. When these two signals (f_s & f_o) are in phase, the frequency of the VCO is locked.

C. Operation (Refer to fig. 15)

The 38-kHz subcarrier in an FM stereo signal is suppressed at the broadcast station, but a 19-kHz pilot signal is transmitted, which MPX Composite Signal is used to control the VCO in the receiver, to reconstruct the 38-kHz subcarrier, to enable the separation of right and left channels, and to activate the stereo indicator (eye).

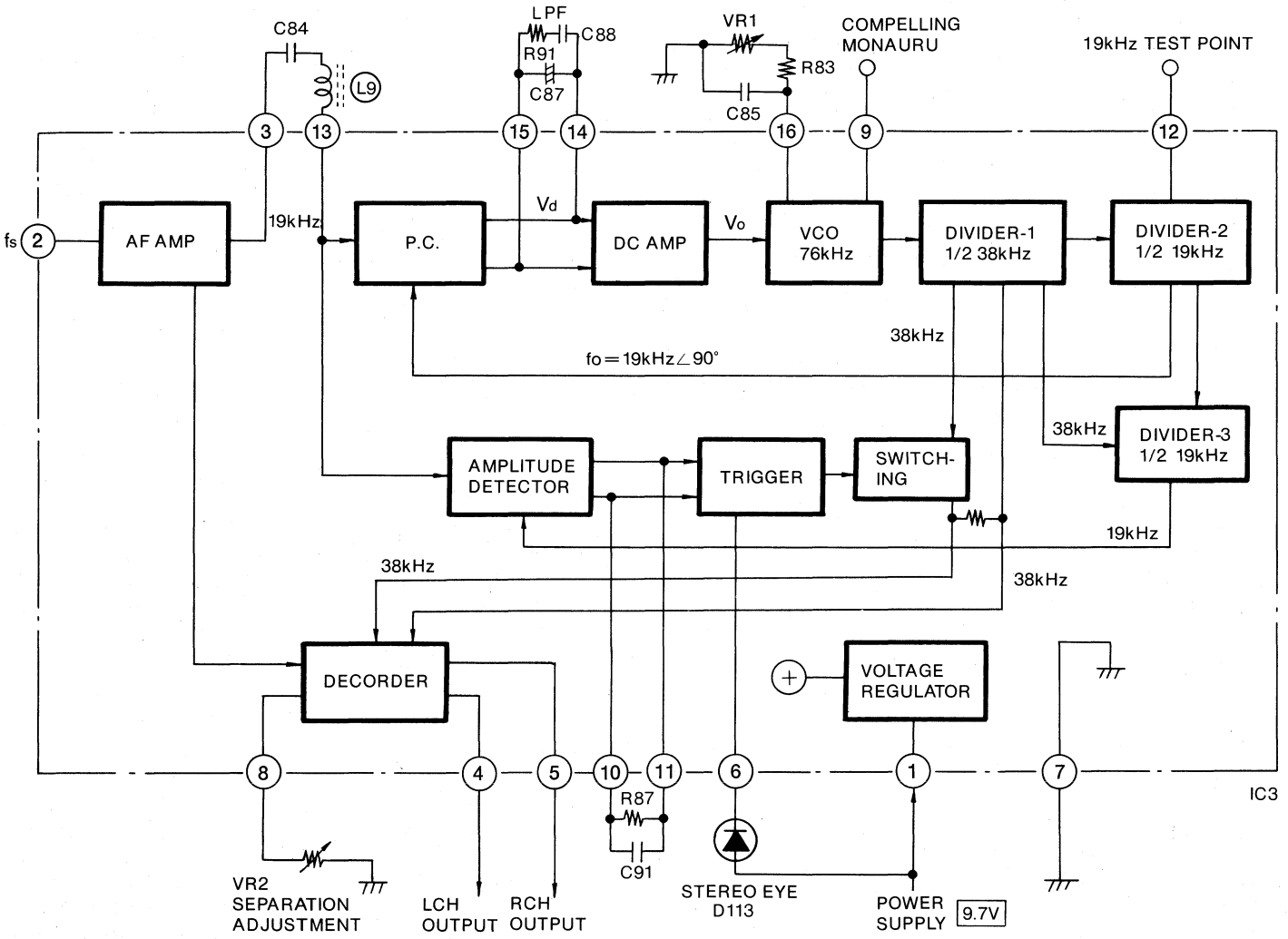


Fig. 15. Simplified block diagram (IC_3)-MPX Decoder.

If the pilot signal (f_s) is not present (as in a mono broadcast) no error voltage (V_d) is applied to the VCO; the VCO output signal (f_o) frequency is not controlled. When the pilot signal is present, it is fed to the PC from the AF amplifier. The PC detects the phase difference, if any, between f_s and f_o and develops a controlling voltage, which is fed to the VCO through the DC amplifier.

The VCO oscillates 76-kHz signal which is cut in half by DIVIDER-1 to obtain a 38-kHz signal. This signal is also fed to the Switching Circuit, and DIVIDERS-2 and 3. DIVIDER-2 cuts the signal in half again, to obtain a 19-kHz signal which is fed back to the PC.

9. INQ (Inpulse Noise Quieting) Circuit

The INQ circuit is used to suppress ignition and other pulse-type noise interference. The main component in this circuit is IC2.

Basic Principales

As shown in the Fig. 17, the gate circuit and capacitor Co remove the pulse-type noise, as follows:

1. When gate is closed, capacitor Co, driven by TR1 (a low-impedance emitter follower) takes on voltage levels that are identical to input signal Vin.
2. When pulse-like noise arrives, the gate immediately opens, and Co "holds" the voltage level imposed immediately prior to arrival of the noise pulse.
3. After the noise pulse passes the gate input, the gate closes, and allows the signal once again to reach Co. Co continues to track the output signal (Vout), but as shown in Fig. 17, the noise pulse is suppressed.

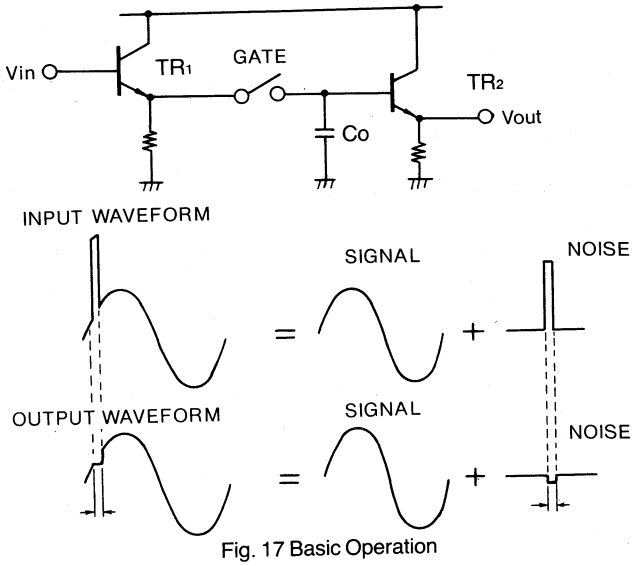


Fig. 17 Basic Operation

INQ control circuit

When power is supplied, the INQ is on; pushing the INQ switch (S6) switches it ON and OFF.

1. When the power is ON, output Q of the J-K flip-flop becomes L, and switching transistor Q11 is in the OFF condition. At this time, the INQ indicator LED (D132) illuminates.
2. Because Q11 is OFF, the INQ IC is not affected by this transistor, and performs ordinary operation. In other words, the INQ changes to the ON (operational) condition.
3. In this condition, pushing the INQ switch (S6) once, changes the output Q from L to H, and Q11 switches ON. At this point, the INQ indicator LED turns OFF.
4. When Q11 switches ON, and a noise pulse appears at point Ⓑ Fig 18, the pulse is grounded through C65. In this condition, IC2 will not operate the INQ. In other words, the INQ changes to the OFF condition. (Refer to the operation explanation of the INQ.)

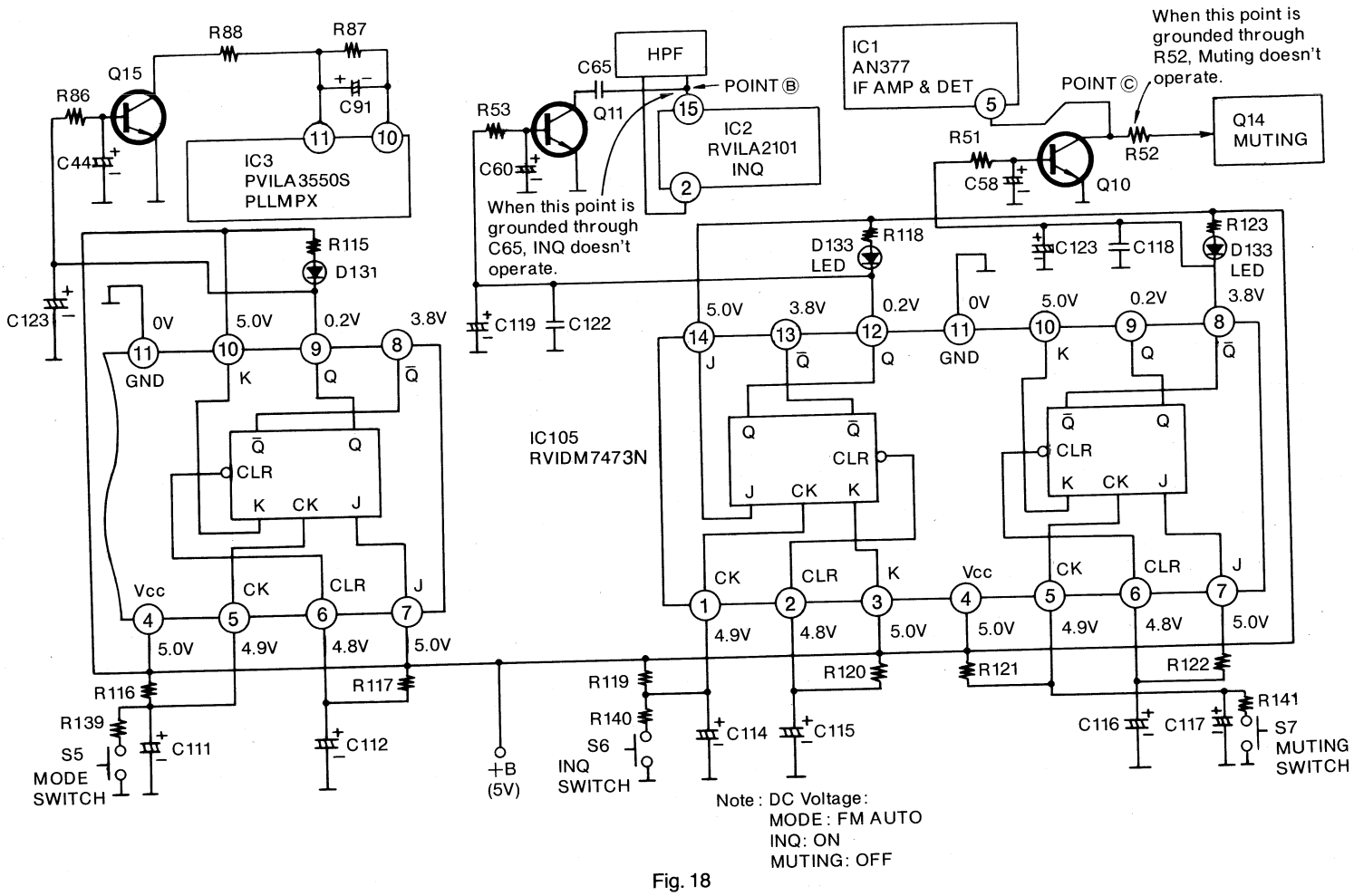


Fig. 18

General

The I N Q circuit is composed of a monolithic integrated circuit (IC2, part no. RVILA2101) and CR filters.
When the input signal with noise is applied to the buffer, it is divided to a low-frequency signal (audio signal) and high-frequency signal (noise) by the low-pass filter (delay circuit) or the high-pass filter.
The audio signal is applied to the gate. Also, the noise is detected, then they are applied to the gate as a gate pulse through the monostable multivibrator.
The gate cuts off the audio signal for a moment when the gate pulse is applied. The audio signal is delayed about 6-μsec, to meet the timing of the gate pulse, by the delay circuit (low-pass filter).
The gated audio signal is amplified and it is sent to the FM stereo demodulator or the AF amplifier as an output signal.
The pilot signal generator circuit and the memory circuit are provided to compensate the FM 19-kHz pilot signal.
For the noise A.G.C., the trigger pulse of the monostable multivibrator is detected and controlled (noise A.G.C.) as the frequency of occurrence of noise increases. This feedback is applied to the noise detection circuit to prevent the gate from cutting off the audio signal during the beat noise (white noise) input.

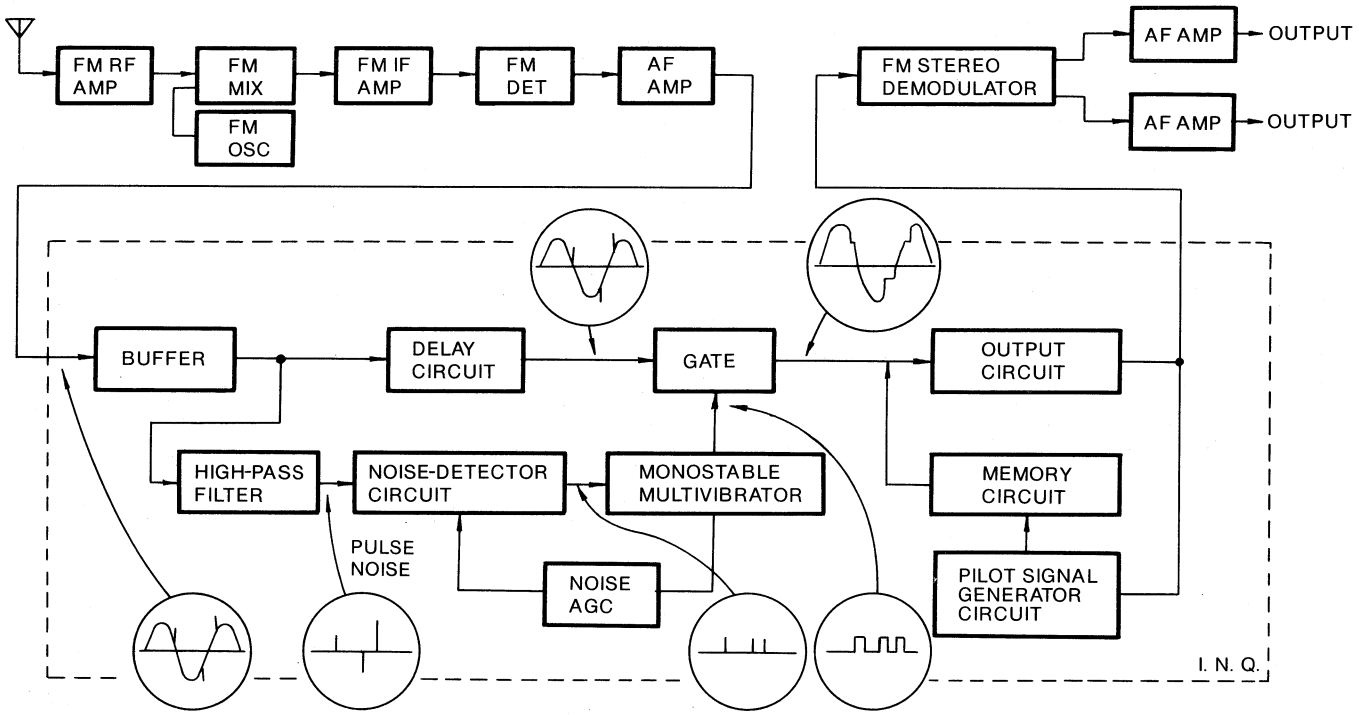


Fig. 19

Buffer

The Buffer is an emitter-follower to invert the impedance.

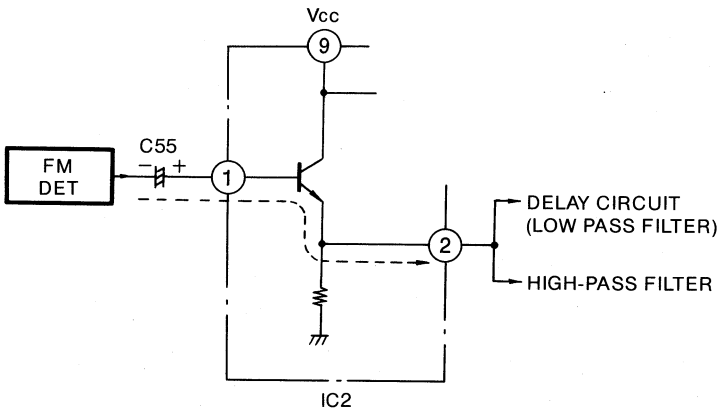


Fig. 20

Delay Circuit (Low Pass Filter)

The audio signal must be applied to the gate at the correct time to insure proper noise blanking.
The delay circuit, used in conjunction with the low pass filter, will delay the audio signal abt. 6 μ sec. in order to compensate for timing pulse delays. Therefore, the audio signal and the timing pulse reach the gate at the correct time.
Using this filter, the amplitude characteristic and delay time are flat with respect to the frequency.

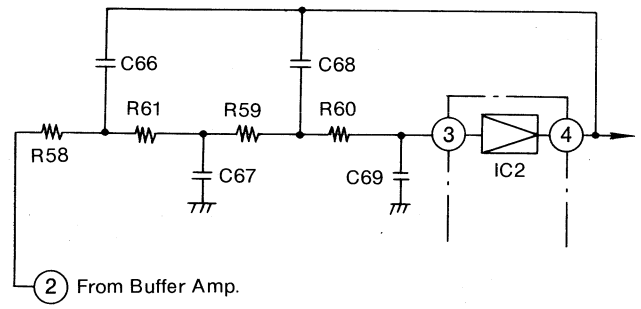


Fig. 21

High-Pass Filter

The high-pass filter, shown in Fig. 22, functions only to pass frequencies higher than the stereo composite signal. This is provided to prevent misoperating the Noise Detector Circuit by the audio signal. This filter has rapid attenuation characteristics in frequencies below the band range. [See Fig. 22 (A) and (B)]

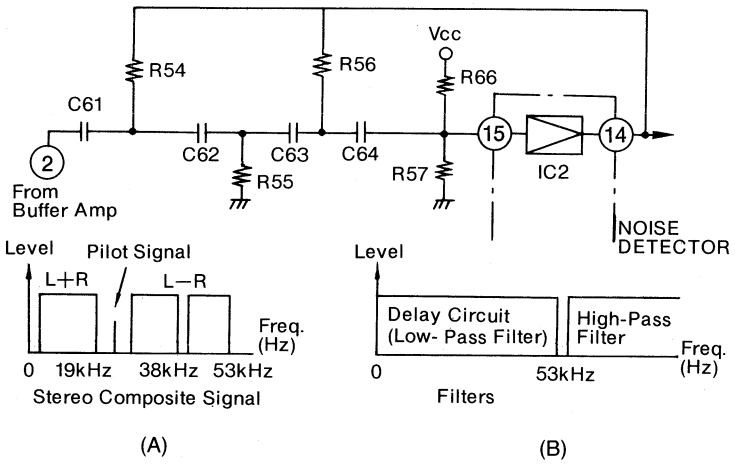


Fig. 22

Noise-Detector Circuit

As shown Fig. 23, the noise detector is composed of a comparator. When the difference of potential between both collectors exceeds the noise-detection level, it detects the presence of the noise.
Capacitor C71 smooths the noise-ripple. When R63=0, noise sensitivity is at its the best, and detection even of small amount of noise is possible.
If, however, noise sensitivity is to higher than necessary, slight noises other than pulse-like noise will be detected, thus result in worsening of the signal/noise ratio. For this reason, the optimum level is determined by the radio's internal noise level.

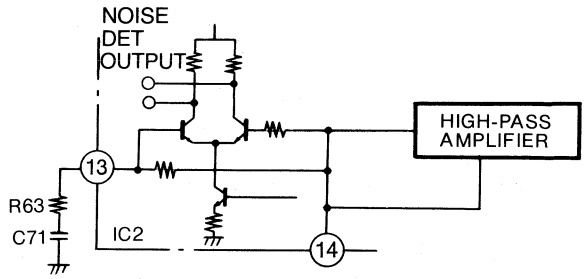


Fig. 23 Noise-Detector Circuit

When pulse-like noise pass through the high-pass filter, the low-frequency range is attenuated and the output signal wave form from the high-pass filter becomes (2) in Fig. 24.
The noise detector detects this signal at a level higher than the noise detection level, and, for pulse amplification, the output becomes pulse lines such as shown (3) in Fig. 24.
When the amplitude of the noise pulse is large, the "lingering", which exceeds the noise-detection level continues for long time, and causes the output pulse lines to become longer. When, on the other hand, the amplitude of the noise pulse is small, the pulse lines become short.
The gate time of the monostable multivibrator is proportional to the pulse lines, the longer the lines, the longer the gate time.
The noise pulse which passes through the low-pass filter becomes a lingering integral wave form after the high frequency falls away, and, when the amplitude of noise becomes great, the energy of the lingering part cannot be ignored.
For this reason, the gate time becomes long in proportion to the amplitude of the noise pulse.

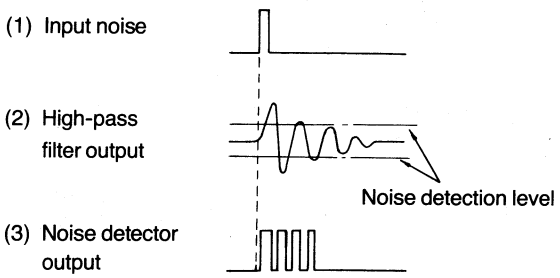


Fig. 24 Pulse Noise Ware Form

Monostable Multivibrator

The monostable multivibrator consists of a combination of a zener diode and a Schmidt trigger. It is designed to produce the control pulse to open the gate for the necessary time according to the output of the noise detector.

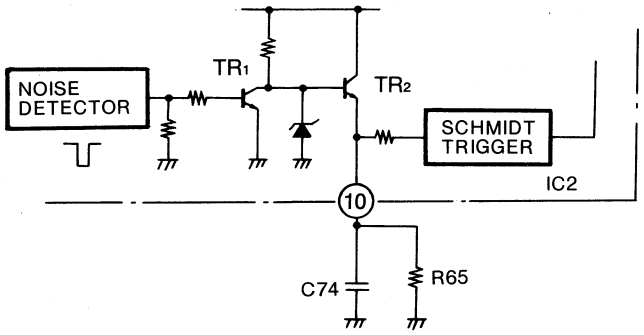
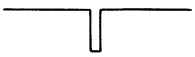


Fig. 25 Monostable multivibrator basic circuitry

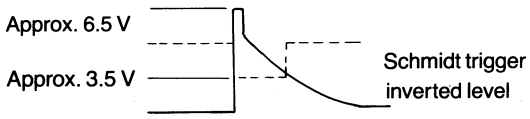
When a negative-going pulse, corresponding to the noise, is applied to the base of TR_1, it turns TR_1 off. The voltage on pin ⑩ of IC_2 increases to about 6.5 V, (set by the zener diode, and C74).
When there is no input from the noise detector, TR_2 turns off, and TR_1 turns on. Capacitor charge becomes discharged because of C74.

(3) in Fig. 26 show the output pulse from monostable multivibrator. The width of the pulse depends on the time constant of C74 & R65.
These operations are shown as an example. In this case, the output of the noise detector is a single pulse.
In an actual case, pulse lines from the noise detector circuit are more than one ((1) in Fig. 26B). The next pulse in a series is applied before the Schmidt trigger reaches the invert level, therefore, the wave form on Pin 10, IC2, will be (2) in Fig. 26B and output from schmidt circuit will be (3) in Fig. 26B.
In other words, as the pulse line output of the noise detector becomes larger, the width of the output pulse (gate time) of the monostable multivibrator increases and it opens the gate for a period of time long enough to cut the pulse-like noise from the audio signal.

(1) Trigger (from noise detector)



(2) Pin ⑩ waveform



(3) Monostable multivbibrator output

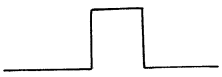
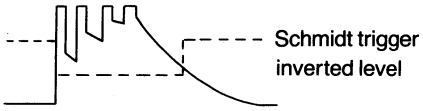


Fig. 26A Monostable multivibrator basic waveforms

(1) Trigger (from noise detector)

(2) Pin ⑩ waveform



(3) Monostable multivibrator output

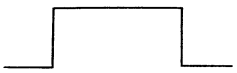


Fig. 26B Monostable multivibrator actual waveforms

Noise AGC

The noise AGC Circuit functions to gradually reduce the noise detection ability as the frequency of occurance of noise increases. When white noise increases in a medium-weak electric field, the white noise causes the gate to open frequently, and, it will cut the audio signal more often. Then the signal/noise ratio becomes worse. It is for this reason that negative feedback is applied to the noise detector when white noise increases in a medium-weak electric field, so that only pluse-like noises which are relatively great are detected.

Gate and Output Circuit

The gate is controlled by the pulse from the monostable multivibrator. It acts like a switch (TR_2) shown in Fig. 27.
When the noise appears, TR_3 turns on, and TR_2 turns off.
When TR_2 turns off, there is almost no charge/discharge on C70 because the base side of TR_4 is high impedance, and the voltage level is maintained at that immediately prior to TR_2 becoming off. While TR_2 is tumed off the audio signal (From the Delay Circuit) does not appear from the output terminal ⑥ IC_2.
When there is no noise, the audio signal from the Delay Circuit appears at terminal ⑥ output after passing through TR_1, TR_2, TR_4 & TR5.

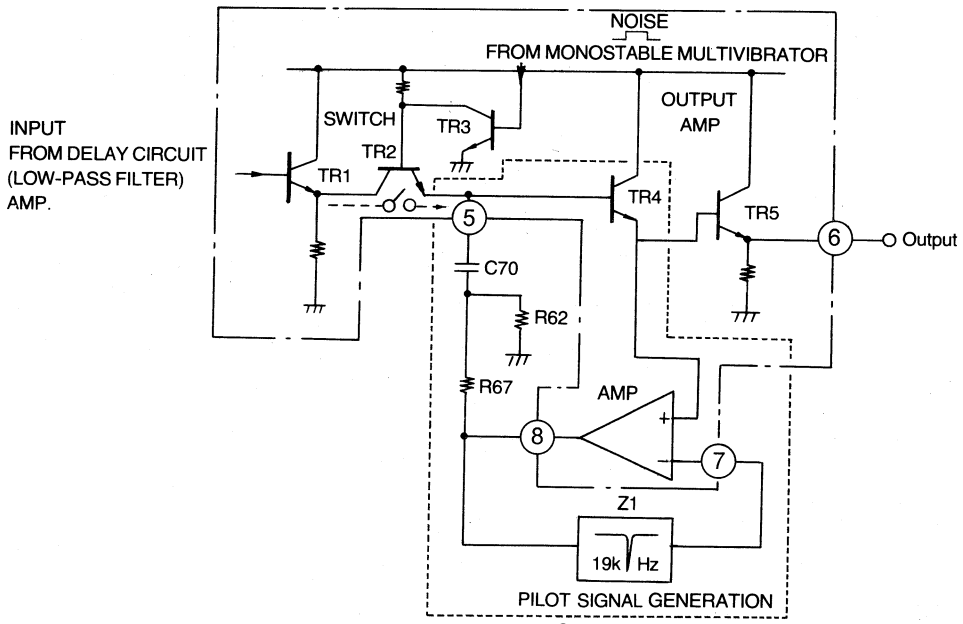


Fig. 27 Gate, output, pilot-signal-generation basic circuits

Pilot-Signal-Generation Circuit

When stereo signals are cut off by the gate during a noise pulse, the stereo pilot signal cannot get through and distorts stereo composite signal. This type of distortion is caused by the presence of the pilot signal even when there is no stereo signal. When there is no stereo signal or when the signal is weak, the pilot signal appears to be relatively strong.
In order to eliminate this type of distortion, a pilot-signal-compensation circuit is used during the time that the gate is open. A 19-kHz sinewave pilot signal is generated (amplitude and phase syncronized by a separate circuit), and superimposed on the voltage on capacitor C70 (See Fig. 28).
The oscillation system is used for generation of the pilot signal at IC_2 (RVILA2101).
During the time that the gate is closed, the amplitude and phase of the pilot signal are memorized, and, when the gate opens, the oscillation of the sine wave with the initial value of 19 (kHz) begins.
If there is no pilot-signal-generation circuitry (Fig. 28A), the condition of noise generation (when the gate opens under no-signal condition) is indicated.

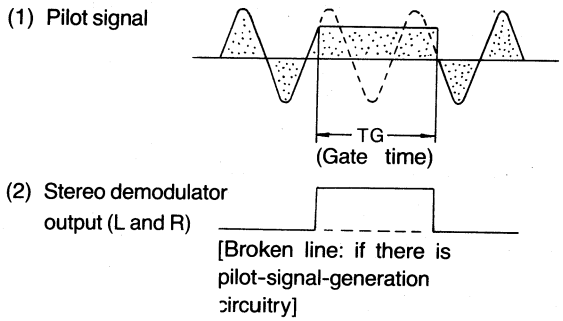


Fig. 28A Noise generated under stereo no-signal condition

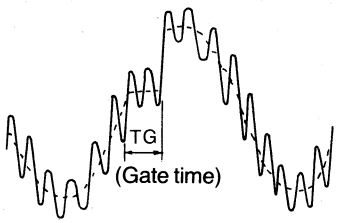


Fig. 28B Output waveform of pilot-signal-compensated. (when L=R)

The pilot-signal-generation circuitry generates a 19-kHz sine wave signal for compensation during the time that the gate is OFF, and the phase and the amplitude of this 19-kHz sine wave must at this time be in agreement with the original pilot signal.
The pilot-signal-generation block in figure 27 has the feedback and selectionability to oscillate the 19-kHz sine wave when the gate becomes OFF. And, if the gate is ON, one edge of that feedback loop is alternately grounded (emitter follower TR_1), stopping the oscillation.

10. Muting and Noise Reduction Circuit

Muting control circuit

When power is supplied, muting is OFF. Pushing the muting switch (S7) switches it ON and OFF.

1. When the power is ON, output $\overline{Q}$ of the J-K flip-flop becomes H, and switching transistor Q10 is in the ON position.
2. Because Q10 is ON, the muting control voltage from IC1 [point ⓒ in figure 29] is forced to decline, preventing normal muting operation.
   In other words, at this time the muting switches OFF.
3. When muting is on, and the switch (S7) is depressed once, the output $\overline{Q}$ goes from It to L, and Q 10 switches OFF.
4. Because Q10 switches OFF, the muting control voltage from IC1 is not affected by this transistor, and is added to the base of muting transistor Q14, performing normal muting control operation. In other words, muting operation is ON.
5. In this way, pushing the muting switch (S7) switches muting operation ON and OFF.

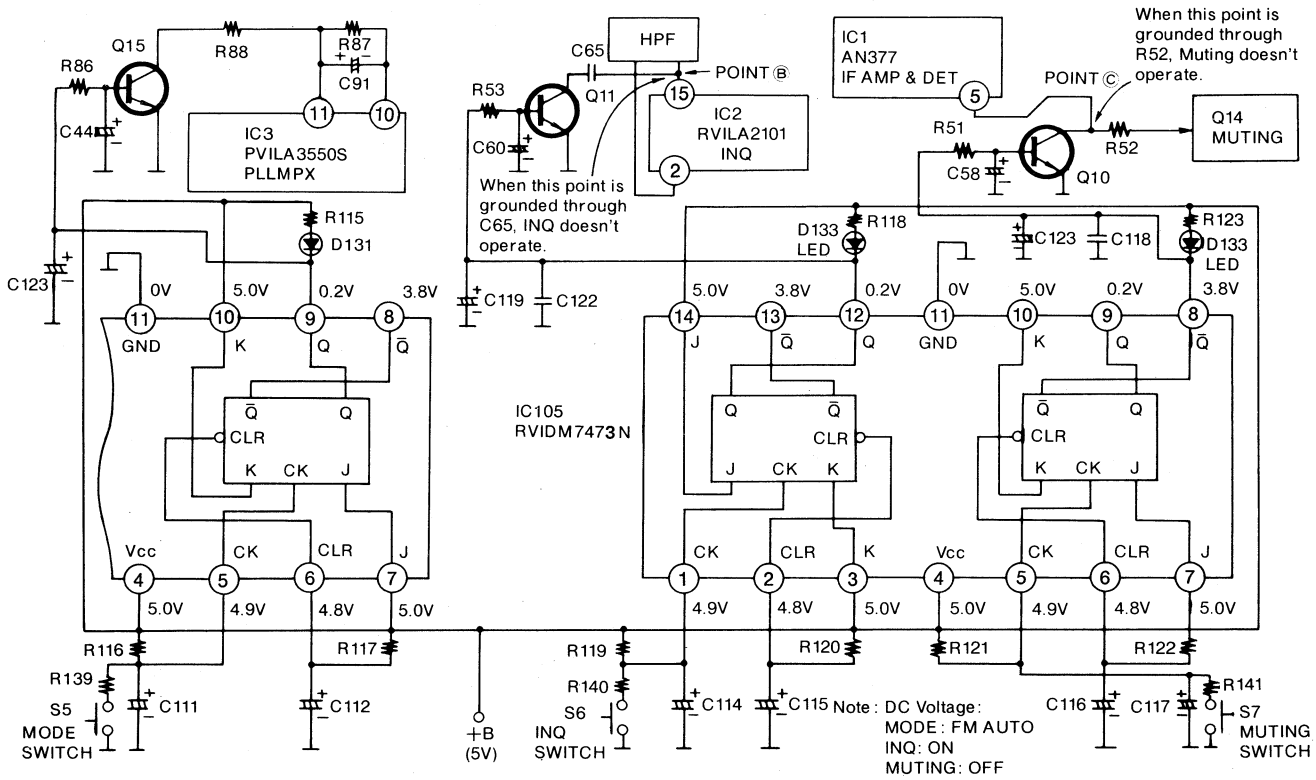


Fig. 29

Treble-range "cut" system

●When the input signal is less than about 30 dB, the control voltage [IC1, AN377 terminal ⑬] of the IF stage correspondingly decreases, and Q13 turns ON. (See Fig. 30.)

●Ordinary signals pass from the input, through R69 and R74, through Q12, and then applied to the input of the MPX. When Q13 is ON, a filter (formed by R69 and C77) attenuates the treble range.

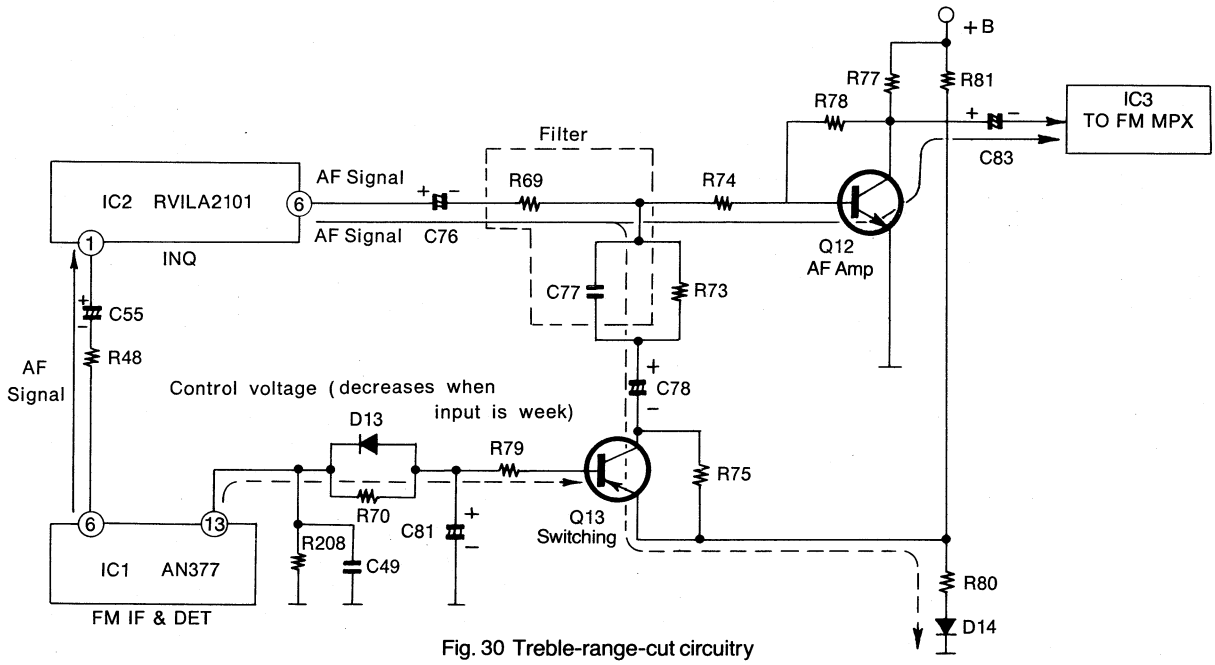


Fig. 30 Treble-range-cut circuitry

AF Output level-reduction system (half muting)

If the input signal drops still more, the voltage from pin ⑫, IC1 increases and applies a more positive voltage on the base of Q14 through R90.

Q14's collector-emmiter impedance decreases and allows some of the audio signal going to the FM MPX to be bypassed to ground through Q14.

As a result, the signal applied to the FM MPX is lower in level than under normal signal condition.

When the input level decreases, the base potential of Q14 increases to the level which is set at R90 and R71. At this time, the level of the AF signal from Q12 decreases approximately 6 dB.

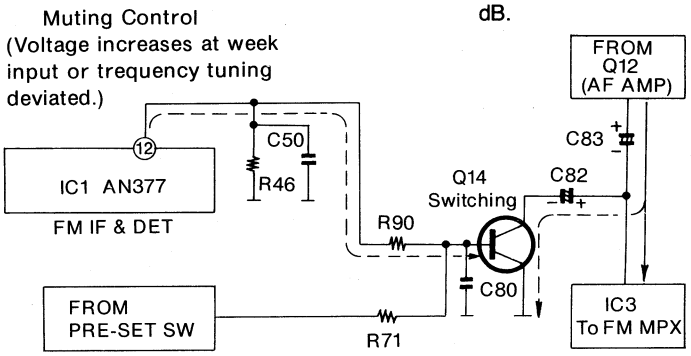


Fig. 31 AF level-reduction circuitry

Muting circuit when power to the unit is switched on.

This muting circuitry has been provided in the RM-610 to cut noise when power to the unit is switched ON.

1. Figure 32 shows the muting circuit when power to the unit is switched ON. A voltage of 13.8 V will appear at terminal ① (B_O) of connector CN3 when power is switched ON.
2. This voltage is differentiated by C60, and the positive side pulse switches Q15 (Q14) ON.
3. Because Q15 (Q14) is ON, the signal from the AF amplifier, Q3 (Q4) passes through Q15 (Q14) and is grounded, preventing discharge of the output.
4. In other words, at this time the AF signal becomes muted.

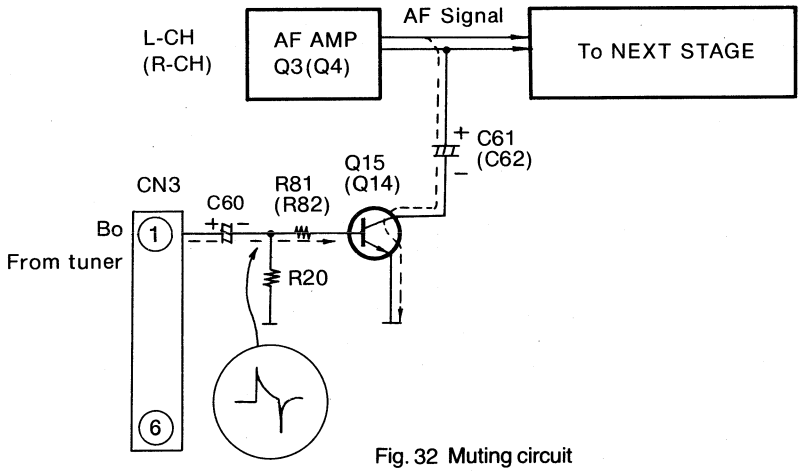


Fig. 32 Muting circuit

11. Level Meter

The LED level meters indicate the output level by using a total of ten LED's, five each for the left channel and five each for right channel.

As shown in the figure below, after being amplified one stage at Q11 (Q12), the output signal is rectified at D1 (D2). The rectified signal is then added to pin (4) of LED indicator drive IC101 (IC102), RVIM51903L.

The LED's illuminate according to that input voltage level.

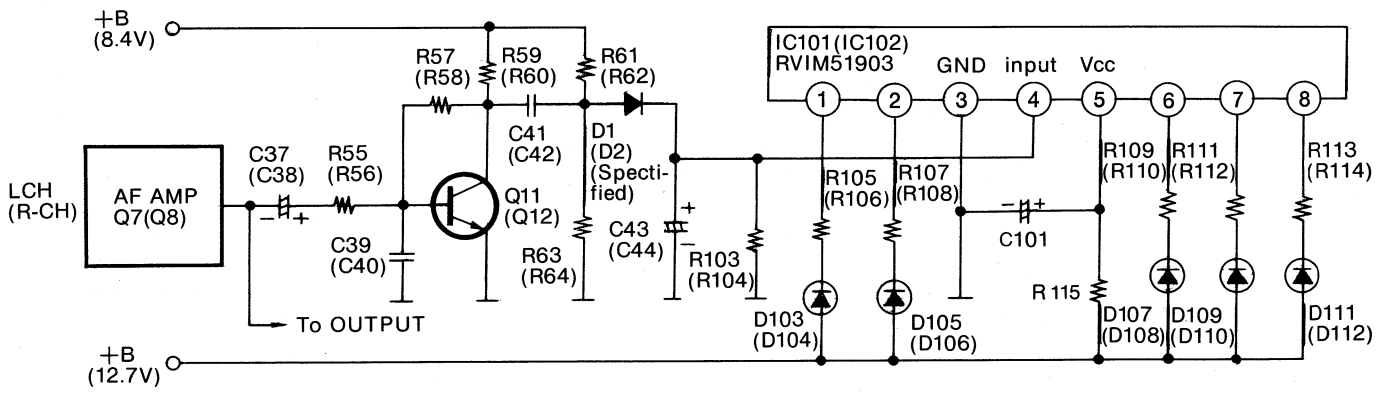


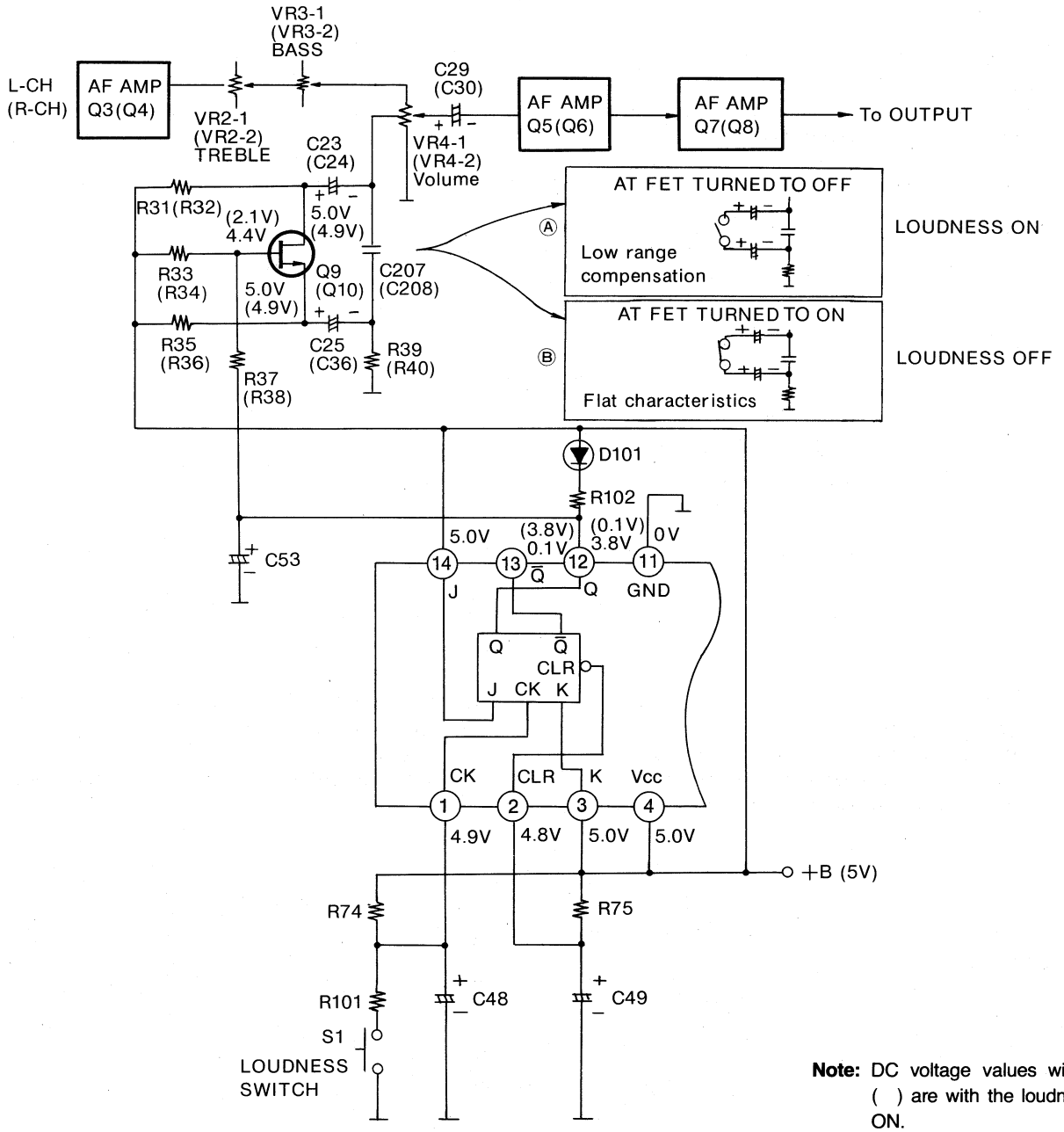
Fig. 33

12. Loudness Control Circuit

The loudness control is operated by a J-K flip-flop, in the same way as the mode, INQ, and muting controls. Actual loudness is switched ON/OFF by an FET switch.

> When power to the unit is switched ON, loudness is ON. Pressing the loudness switch (S1) switches loudness ON and OFF.

1. In the circuit shown in figure 34, when the power souce is turned on, the output "Q" of the J-K flip-flop becomes "L" therefore the gate voltage of the FET switch Q9 (Q10) becomes low level, and Q9 (Q10) is off at this time.
2. When Q9 (Q10) is off, the source-drain interval of Q9 (Q10) is opened, so it can be expressed by equivalent circuitry such as shown in Fig. 34 Ⓐ .
3. As can be seen in the circuit shown in Fig. 34 Ⓐ , the mid- and high range is decreased by C207 (C208) to the level set by R39 (R40), and, as a result, the low range becomes the increased frequency response.
4. In other words, the loudness is ON at this time.
5. If the loudness is on, and S1 is pressed once, the output "Q" of the J-K flip-flop changes from "L" to "H", and Q9 (Q10) turnes ON.
6. When Q9 (Q10) is ON, the electrolytic condenser is connected in parallel with C207 (C208), and this becomes the circuit shown in Fig. 35 Ⓑ .
7. In the circuit shown in Fig. 34 Ⓑ , the electrostatic capacity of the electrolytic condenser is set very big compared to C207 (C208), and, for that reason, the AF signal frequency response becomes flat to the level determined by R39 (R40).
8. In other words, the loudness is OFF at this time.
9. In this way, each time the loudness switch (S1) is pressed, the loudness becomes ON and OFF alternately.



Note: DC voltage values within ( ) are with the loudness ON.

Fig. 34 Loudness-control circuitry-Preamp

(13) Dolby Noise-Reduction System

Dolby noise-reduction IC, RVIHA1126 is used in this cassette deck. This integrated circuit contains the Dolby noise-reduction system for two channels.
The RM-610 uses the Dolby noise-reduction system for playback only (recordings cannot be made).

Dolby Circuit Operation

Block Diagram

The Dolby noise-reduction IC block diagram is shown with a listing of terminal functions.

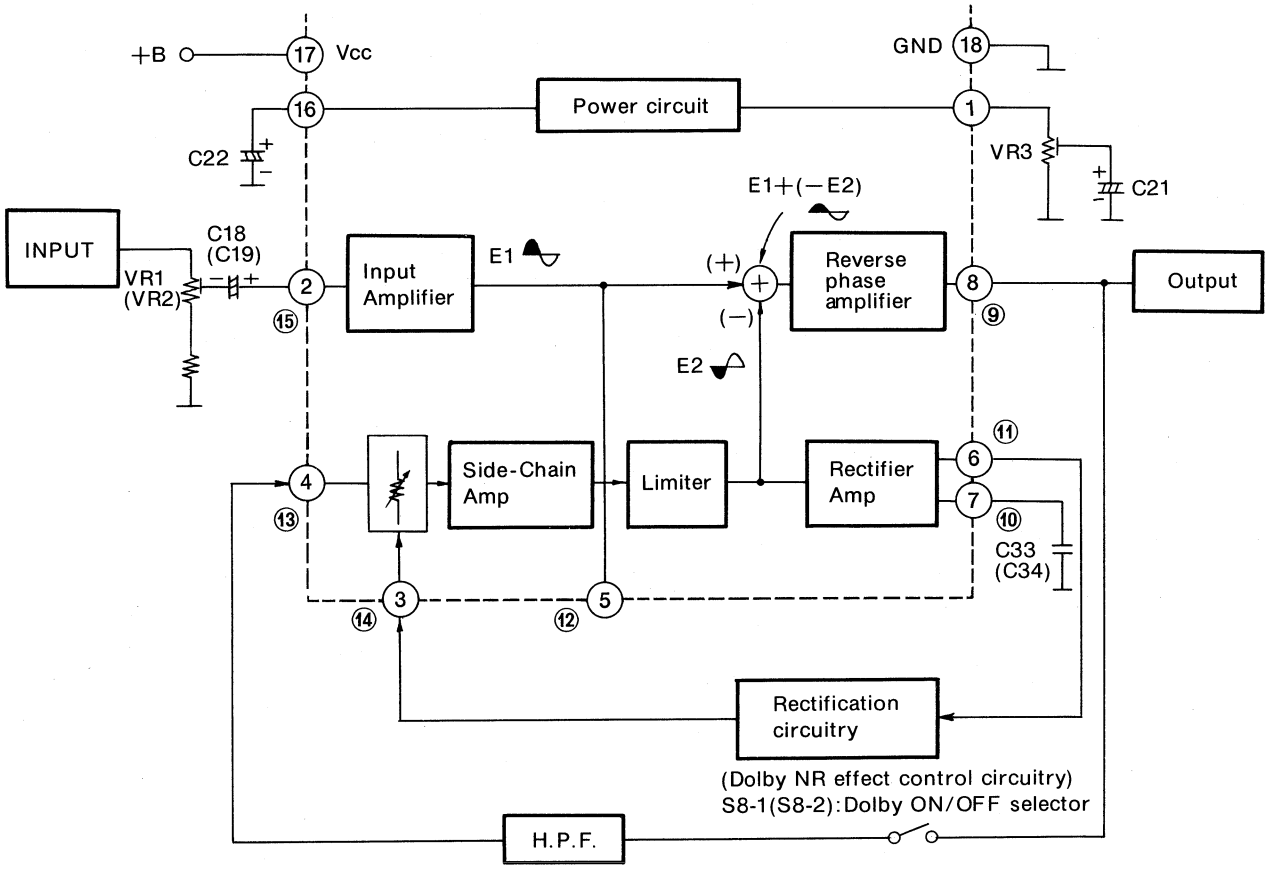


Fig. 35 Block Diagram-IC3 RVIHA11226 (Casstte Deck)

Notes: 1. Function of each terminal

- ①: Dolby NR operation control input
- ②, ⑮: AF signal input
- ③, ⑭: Input for Dolby NR control
- ④, ⑬: Input from H.P.F. (High-Pass Filter)
- ⑤, ⑫: Output (for Dolby NR recording use)
- ⑥, ⑪: Output for Dolby NR control
- ⑦, ⑩: For connection of by-pass capacitor of rectifier amplifier
- ⑧, ⑨: Dolby NR handling signal output and output to H.P.F.
- ⑯ : Dolby NR operation standard voltage
- ⑰ : IC power input
- ⑱ : Ground

2. Function of each volume
   VR1: To designate the Dolby point
   VR3: To designate Dolby NR operation

Dolby Playback Operation

In the Dolby B record process, low level signals in the middle and high frequency range are amplified and added to the main signal input. When this process is applied during recording, the input signal becomes less susceptible to the addition of noises. In order to attain the Dolby noise reduction effect, these amplified signals must be attenuated in the playback mode.
The Dolby noise reduction IC is used as a playback processor. It's function is to attenuate the middle and high frequency range signals that are amplified during the record process.
The playback signal from the pre-amplifier is applied to the integrated circuit at terminal②. This signal (E1), is applied to the reverse phase amplifier after passing through the input amplifier. The input signal (E1), passes through the reverse phase amplifier and is then divided into 2 paths. One signal path is applied to the AF circuit as the output signal, while the second path is applied to the high pass filter as the control signal (-E2). The control signal follows a path through the high pass filter, variable resistance, side chain amplifier, and limiter. The output of the limiter (-E2) is applied to the reverse phase amp.
At this time, the control signal (-E2) is applied to the rectifier circuit after passing through the rectifier amp.
The rectifier circuit is used to smooth the control signal to a positive DC level. This level will control the variable resistance in response to level fluctuations of the control signal (-E2).
The output of the limiter is dependant upon the variable resistance and the frequency response of the high pass filter. These conditions are directly related to the level of the control signal (-E2). When the output of the limiter is applied to the reverse phase amp, attenuation of the output signal is obtained.
As a result of the above conditions, the control signal (-E2) can equalize the Dolbyized signal (E1), and pass the output signal E0=E1+(-E2).
The Dolby selector switch will break the path of the control signal (-E2) when in the "Dolby Out" position. This will open the side chain loop and cancel Dolby noise reduction.

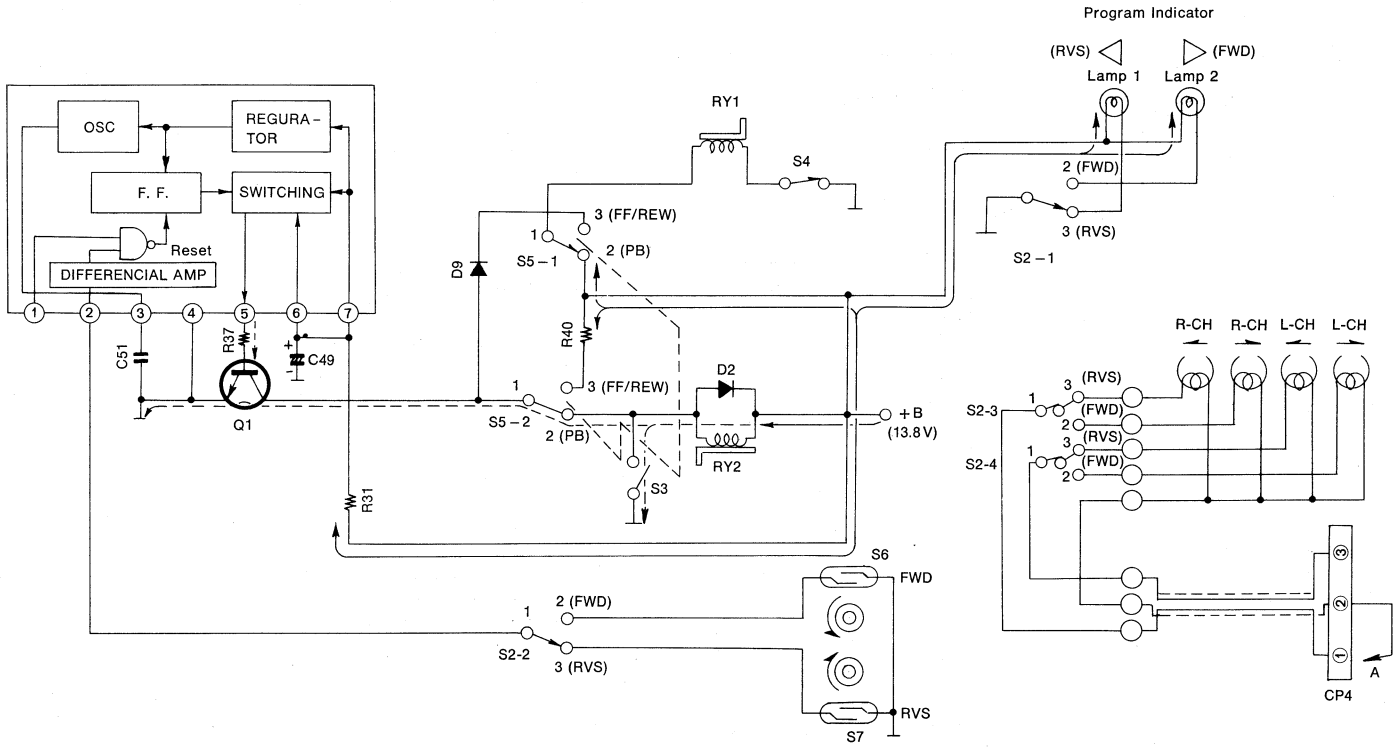
14. Automatic-Reverse Control

Electrical

This cassette deck section has both automatic-reverse and manual-reverse functions. The automatic-reverse function uses integrated circuitry (AN6249) especially for this purpose.

An outline of this function follows:

1. Reed switch S6 or S7 stops turning on and off when the reel table stops. This stoppage signal is applied to pin ②, and detected.
2. After the time (T=3.6×C51) determined by the value of capacitor C51, has passed, one pulse signal is generated from pin ⑤, and switches transistor Q1 ON.
3. Plunger RY2 (for reverse) is attracted, and S2 changes position.
4. Each time RY2 plunger is attracted, the mechanism begins reverse operation.
5. Simultaneously, the automatic-reverse switch S2 switches, the program indicator lamps, the playback head winding and the reed switch.
   (Rotation detection is constantly sensed by the reed switch at the take-up reel table.)
6. If the program is changed manually, by momentarily closing S3, RY2 goes to work, as in 4 and 5 above.



Note: S2-1~S2-4: Auto reverse switch shown in reverse position.
2 . . . . .Forward, 3 . . . . .Reverse
S3: Program switch shown in OFF position.
S4: Eject switch shown in play positio.
S5-1,~S5-2: Playback/FF REW switch shown in playback position.
2 . . . .Playback, 3 . . . . .FF/REW
S6: Tape end detector switch (Forward)
S7: Tape end detector switch (Reverse)
RY1: Plunger for holding cassette
RY2: Plunge for reverse (program change)

Fig. 36 Automatic-reverse and automatic ejection control circuitry

Automatic-Reverse IC (AN6249). (Figs. 36 and 37.)

After the tape is fully wound (after the take-up reel table stops rotating)

Pin ① of AN6249 is always set at H (high) level. When a pulse is not applied to pin ②, the filp-flop starts operation and at the 448th oscillation, generates one pulse. See Fig. 37. This starts reverse operation of the mechanism, by switching output transistor Q1 ON.

When the tape is moving (the reel tables rotating)

The pulse from the reed switch is applied to pin ②. At the falling edge to pulse, the Flip-Flop is reset the each time.

As a result, the waveform count remains at one, and no output pulse is generated.

Notes:

When pin ① is at low level there is no generation of an output pulse from pin ⑤, whether or not the pulse from pin ② exists; therefore, there will be no reverse operation even at the tape end.

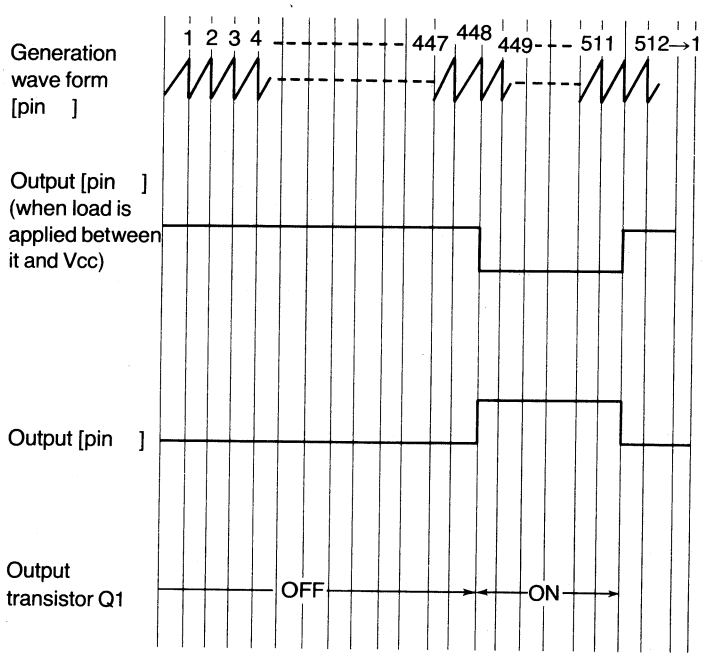


Fig. 37 Output waveform of each pin of AN6249

(B) Mechanism Operation

Tape Playback in Forward Direction [Refer to Figures 38-(A) and (a).]

1. The tape is moved in the forward direction by the pressure roller lever (R) and capstan (R), and wound on reel table (R).
2. The rotation force from the motor to the pressure roller lever (R) and reel table (R) are as follows.
   - ●Transmission route of rotation force from motor to pressure roller lever (R)
     Motor→motor belt→flywheel (R)→capstan→pressure roller lever (R) [transmission of rotation force at contact point ①.]
   - ●Transmission route of rotation force from motor to reel table (R)
     Motor→motor belt→flywheel (L)→intermediate idler [transmission of rotation force at contact point ②]→idler (R) [transmission of rotation force at contact point ③]→reel table (R) [transmission of rotation force at contact point ④.]
3. In addition, reverse gear (A) is rotated at this time by the reverse belt, but, because reverse gear (C) is not meshed with reverse gear (A), there is no effect on forward playback. [As shown in figure 38-(a), meshing of reverse gears (A) and (C) is prevented by the driving lever at contact point ⑤.]
4. In this way, the forward direction playback is maintained.

Reverse Operation

1. As described before, when the tape comes to its end, control is electronic and the plunger for reverse automatically attracts the driving lever, as shown in figure 38-(b).
2. Then contact point ⑤ [figure 39-(a)] is released, and reverse gear (C) moves in the direction of arrow ①, resulting in the condition shown in figure 38-(b).
3. At this time, reverse gears (A) and (C) are meshed, and reverse gears (B) and (C) start rotating in the direction of arrow ②.
4. Projection part (A) of reverse gear (B) starts rotating in the direction of arrow ③ [figures 8-(A) and (b)].
5. As a result, the reverse lever moves in the direction of arrows ④, ⑤ and ⑥, using the pivot (C) as a fulcrum, and projection part (A) moves from position Ⓐ to Ⓑ [figure 38-(A) and (B)].
6. Pressure roller lever (R) moves in the direction of arrow ⑦, with pivot (A) as the center, and the contact with capstan (R) is released.
7. Because idler lever (R) moves in the direction of arrow ⑧, with pivot (F) as the guide, the contact [contact point ③] of idler (R) and the intermediate idler shaft is released.
8. Because the intermediate idler moves in the direction of arrow ⑨, the contact of flywheel (L) and the intermediate idler [contact point ②] is released.
9. By the operations described above, forward playback is released.
10. When projection part (A) of reverse gear (B) comes to position Ⓑ from position Ⓐ, as shown in figure 38-(B):

* Reverse gear (C) is again locked by the driving gear at contact point ⑥, at this time the meshing of reverse gears (A) and (C) are released. (At this time, one cycle of the reverse operation is completed.)
* When the switch lever rotates in the direction of arrow ⑩, with pivot (E) as the center, auto-reverse switch (S2) changes from the forward to the reverse position.

11. When the reverse lever, with pivot (C) as the center, moves in the direction of arrow ⑥ [figure 8-(A)], pressure roller lever (L), with pivot (B) as the center, moves in the direction of arrow ⑫, and subsequently, as shown in figure 38-(C), makes contact with capstan (L) at contact point ⑦ .
12. In figure 38-(A), because the idler lever moves in the direction indicated by arrow ⑬, with pivot (G) as its guide idler (L) makes contact with the intermediate ilder shaft at contact point (8) in figure 38-(C).
13. Simultaneously, idler (L) makes contact with reel table (L) at contact point ⑨ [figure 38-(C)].
14. The intermediate idler moves in the direction of arrow ⑨ in figure 8-(A) as a result of its contact with idler (L), and subsequently, as shown in figure 38-(C), it makes contact with flywheel (R) at contact point (10).
15. Upon completion of all the operations described above, the tape will begin to be sent by pressure roller lever (L) and capstan (L), and the rotation power from flywheel (R) is transmitted to reel table (L) through contact points ⑩, ⑧ and ⑨, and reel table (L) begins to wind up the tape. In other words, the reverse operation begins.
16. In this way, each time the plunger for reverse (RY2) attracts the driving lever (i.e., at the end of the tape, or when the program selector button is pressed), the direction of tape movement is reversed, and reverse operation begins.

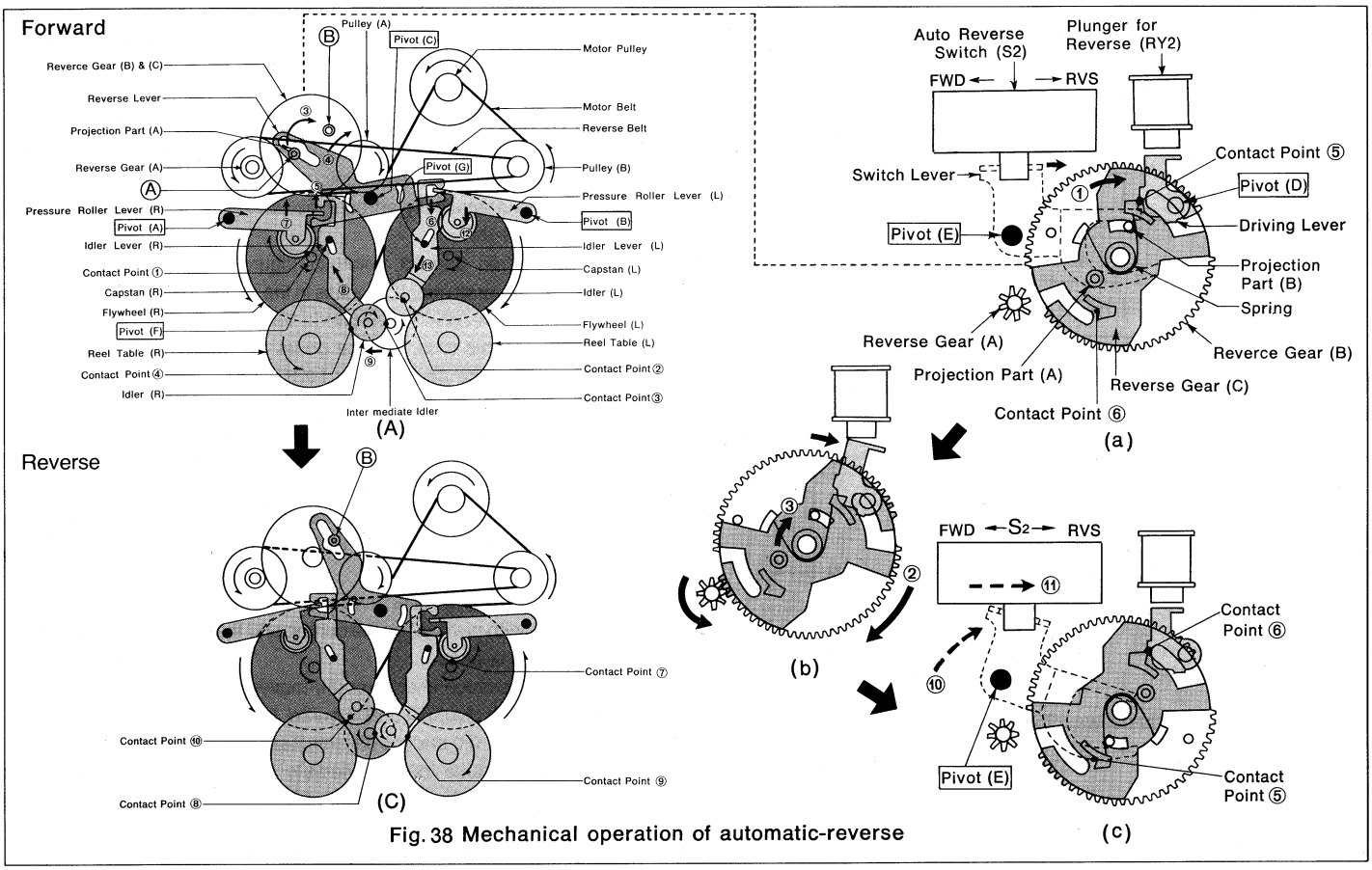


Fig. 38 Mechanical operation of automatic-reverse

5. AUTOMATIC EJECTION CONTROL

When the tape reaches its end during fast forward or rewind, the cassette will be automatically ejected. This is accomplished by using the IC (AN6249) for automatic reverse.

① In the circuitry in figure 36, of section 4, the fast forward/rewind, playback switch S5 is in the 3 ("FF/REW") position during fast forward or rewind. The power is supplied through R40 and D9, RY1 (for cassette hold) is attracted and the connection for fast forward or rewind operation is made.
② When the tape reaches its end, pin ② of AN6249 detects the tape end, in the same way as explained for automatic reverse, so that a positive pulse appears at terminal ⑤ , and Q1 becomes ON.
③ When Q1 is turned ON, the voltage supplied through D9 passes through the collector-emitter of Q1 and is grounded, and turn the power to RY1 off.
④ As a result, the tape cassette is ejected because the attraction of RY1 has been released.

16. Sound Equalizer Model RM-E610

The RM-E610 is available as a separate and optional sound equalizer developed especially for use with the RM-610 "Cockpit" model. This sound equalizer can be used in order to make corrections of the differences in tone quality which appear in different types of cars, and, in addition, it can also be used to create variations of tone quality at the listener's pleasure.
This unit can be used for changing the output by ±12 dB at each of five frequency points: 60 Hz, 250 Hz, 1 kHz, 3.5 kHz and 10 kHz.

Operation outline

Figure 39 shows the block diagram of the model RM-610. It is composed of two-stage AF amplifiers (left and right channels) and five filter amplifiers for each channel, one for control of each frequency point.

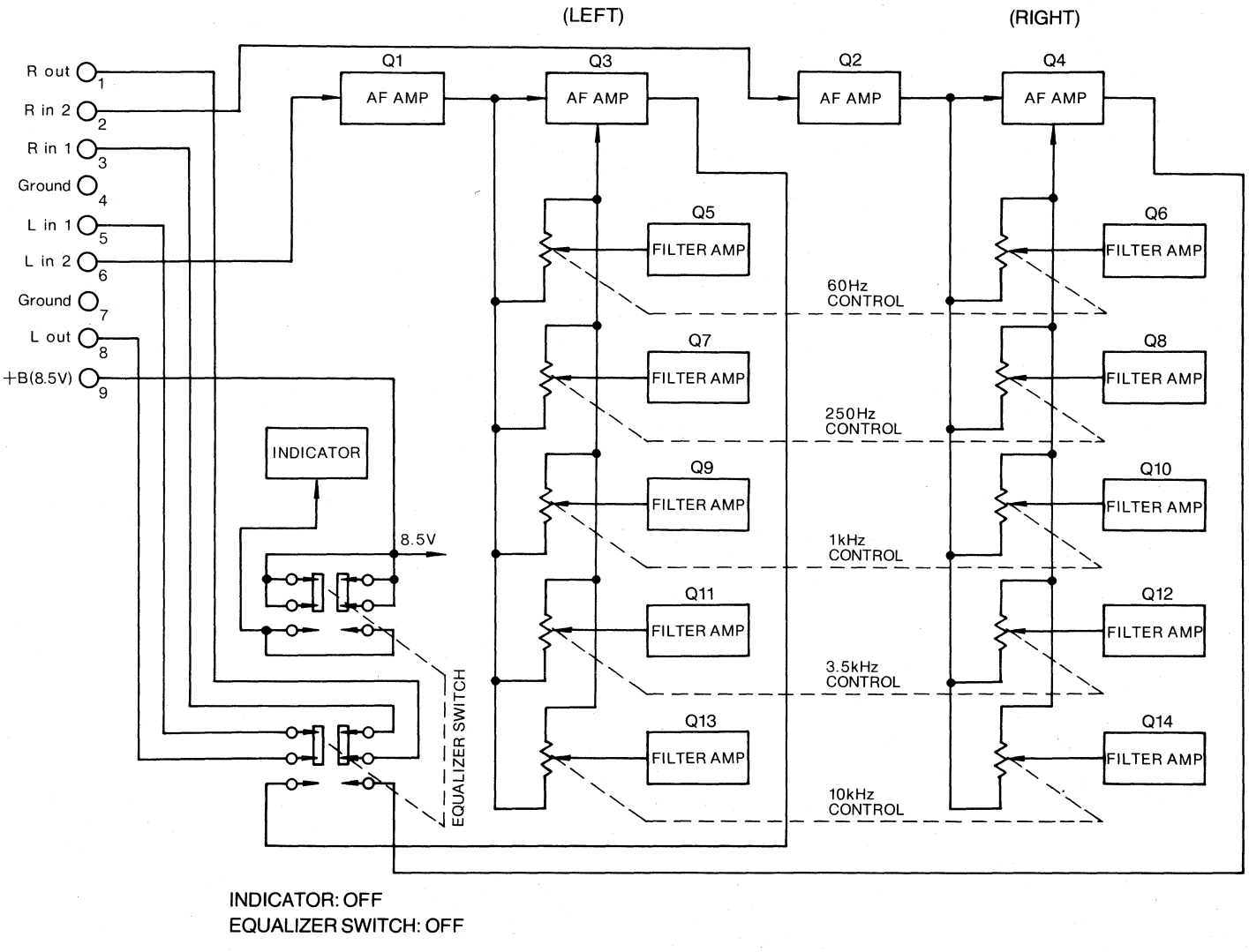


Fig. 39 Block Diagram-Model RM-E610

Figure 40 shows the control circuitry for the 60-Hz frequency point, which will be used for an explanation of actual circuitry operation.
This circuitry consists of 2-stage AF amplification, Q3 and Q4, and filter amplifiers Q5 and Q6. These filter amplifiers are connected via the variable resistance for frequency control, between the base and emitter of Q3 and Q4. As a circuit, it is equivalent to an LCR direct-coupled resonance circuit with a resonance frequency of 60 Hz.

The input impedance seen from the base side of Q3 and Q4 is considered to be Z_b, and the emitter resistance is considered to be Z_e. Next, as shown in the figure, the impedances seen from both ends of VR1 (toward filter amplifiers Q5 and Q6) are considered to be Z_1 and Z_2. The input impedance of the filter amplifier is considered to be Z, and the resistance values from both ends of volume VR1 are considered to be R_1 and R_2.

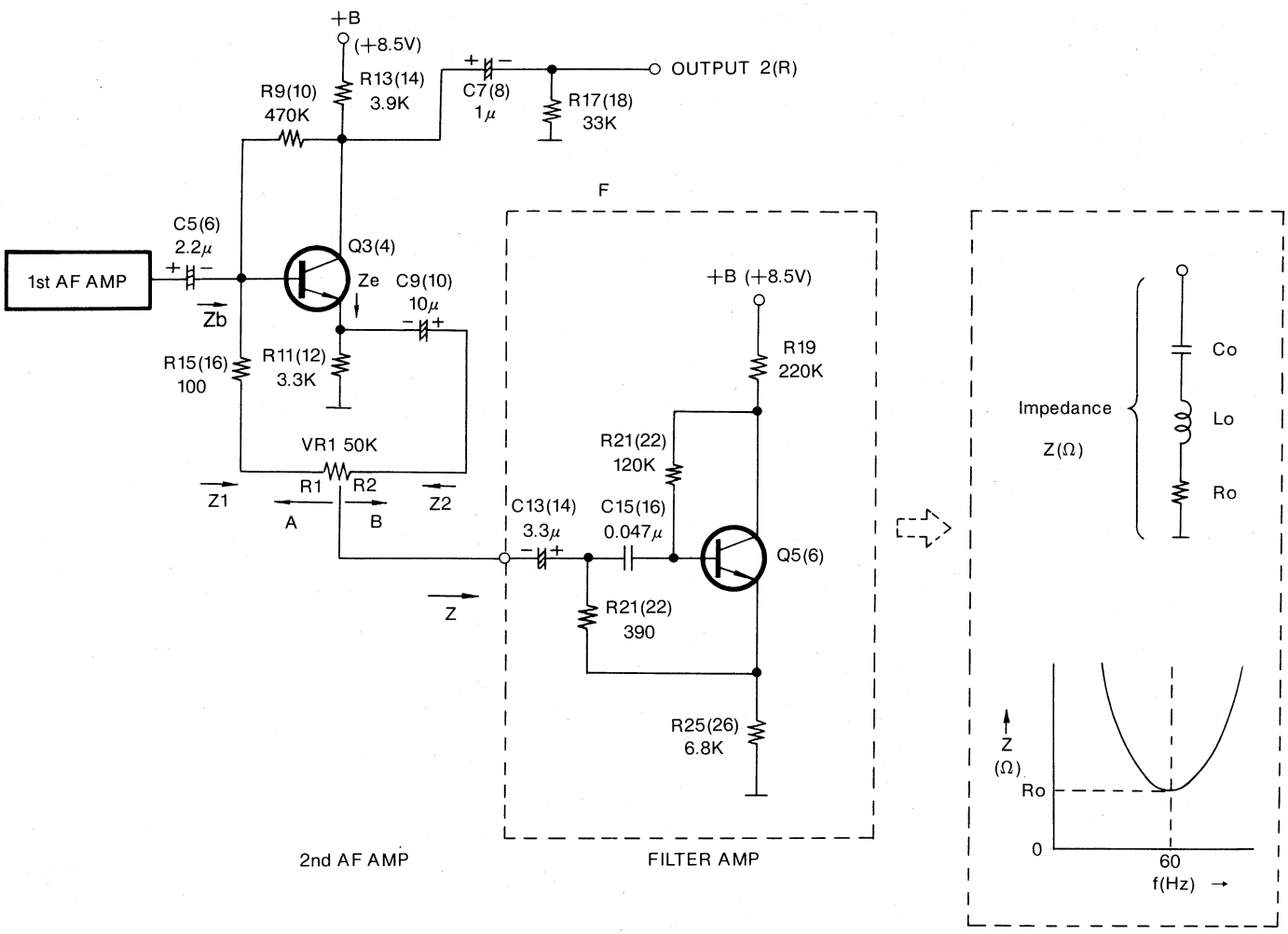


Fig. 40 60 Hz Equalizer Circuit

Fig. 40 Ⓐ

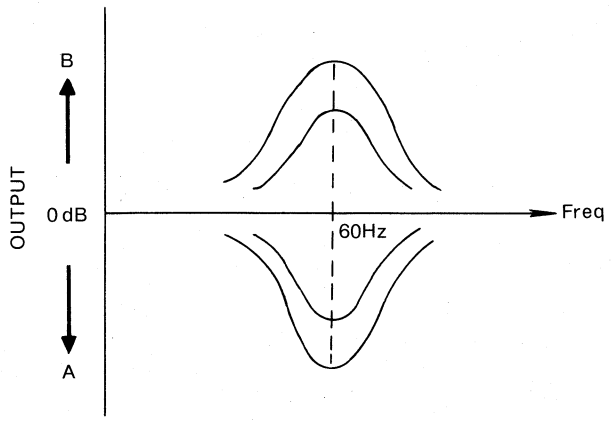


Fig. 41 Output vs. VR_1 Position

When VR_1 at center position

Because VR_1 is at center position, R_1 and R_2 are comparatively high to the impedance Z of Filter Amp, Zb and Ze are not affected by changing of impedance Z.

Therefore, there is no change of the 2nd AF Amp. even at 60 Hz and the frequency response becomes flat.

When VR_1 is moved in direction A

When VR_1 is moved in direction A, impedance of Z_1 becomes less than Zb.

Then the output of the 2nd AF Amplifier decreases. Consequently, as shown in Fig. 41B, the output decreases (maximum decrease at 60 Hz).

When VR_1 is moved in direction B

When VR_1 is moved in direction B, Emitter impedance (Ze) of the 2nd AF Amp. decreases. Then the output (gain) of the 2nd AF Amp. increases (maximum increase at 60 Hz).

The frequency response is controlled at the other frequencies (250, 1 k, 3.5 k & 10 kHz) in the same way.

17. DC-DC Converter

The DC-DC converter is used to boost battery supply voltage (13.8 volts, DC) to 48 volts DC, which is split up so that it is +24 and −24 volts with respect to ground.

1. The DC power from the battery is chopped by Q101 and Q102 to appear as a modified from of AC voltage, to enable transformer action by T1. See Fig. 42.
2. This AC voltage is stepped up, and changed back to DC by the full-wave rectifier, diodes D101, D102, and the filtered by chokes CH101 and CH102, and capacitors C103, C104, C105 and C106.

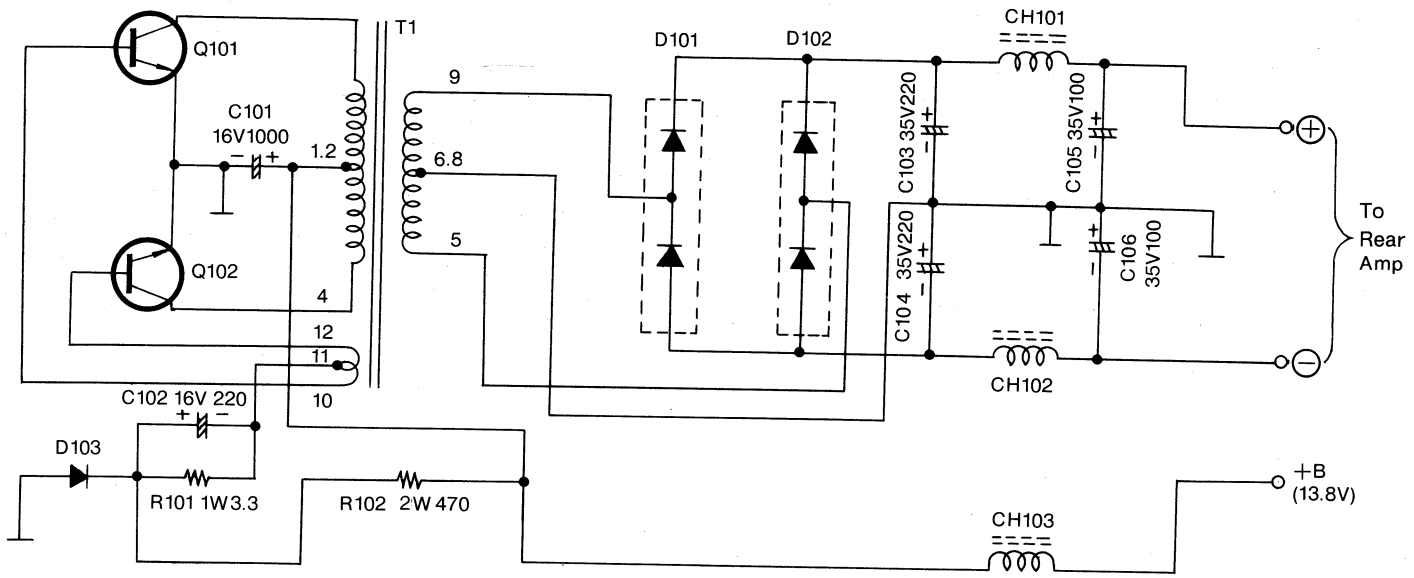


Fig. 42 DC-DC Converter Circuiting

18. BTL (Balanced Transformerless) Circuit

The BTL circuit IC3 (IC4) RVIM51517L, is shown in Fig. 43. It operates as follows:

1. The audio frequency signal is applied to the base of transistor Q10 through the coupling capacitor C31.
2. Two outputs are obtained, one from the collector, which is phase inverted, and one from the emitter which is of the same phase as the input signal.
3. These signals are fed to IC3 (Amp 1 and Amp 2) through coupling capacitors C33 and C35.
4. Both signals are then amplified, and applied across the load R. The addition of these two signals doubles the output signal voltage, which results in a quadrupling of the output power.
   i.e, From Ohms law we know that
   Power=E^2/R
   If E=3 volts and if R=4 ohms, then the power=2.25 watts.
   If E is now doubled to 6 volts, and R remains the same at 4 ohms, then the power will be 4 times greater; at 9 watts.
5. In other words, when a BTL circuit is used, it is possible to get four times as much power as can be obtained from one amplifier.

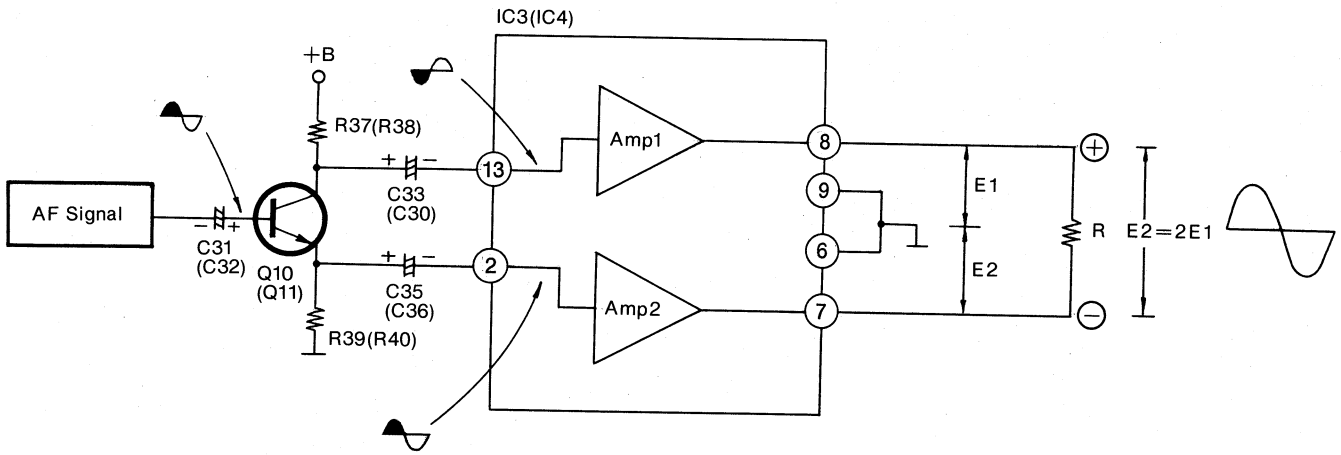


Fig. 43

19. Protection circuit

The RM-M610 includes special protection circuitry to instantaneously release RL1 and stop the power supply if, for any reason, the rear output is short-circuited.

1. In figure 45 transistor Q5 (Q6) will become ON, turning ON transistor Q7, if the output line (point Ⓐ is shorted to earth).
2. When Q7 turnes ON, the gate voltage [point Ⓑ] of the thyrister (SCR1) increases.
3. When the gate voltage becomes higher than the cathode voltage, a short-circuit occurs between the anode and the cathode, and SCR1 turnes ON.
4. When SCR1 turnes ON, the potential from pin ⑦ of the connector is grounded, and, because the base voltage [point (C)] of Q9 (which is ON) decreases, Q9 turnes OFF.
5. When Q9 turnes OFF, current no longer flows to RL1, and, therefore, RL1 is released and power supply is stopped.

20. Power Supply Relay Control Circuit

Because a large current can flow when the power amplifier is turned on, a switching transistor (Q9) and relay (RL1) are employed, as shown in Fig. 44.

1. When the power switch in the FM tuner section is turned on or when a cassette is inserted, 13.8 V is applied to the base of transistor Q9, through connector terminal 7. This causes to conduct and energise relay RL1. When the relay closes, battery voltage is applied to the power amplifier.
2. When the power switch in FM tuner section is turned off when no cassette is inserted, or if the cassette is ejected when the power switch is off, the voltage on terminal⑦and the base of Q9 will drop to zero, and turn Q9 off, which in turn will open RL1 and shut off the power supply current.

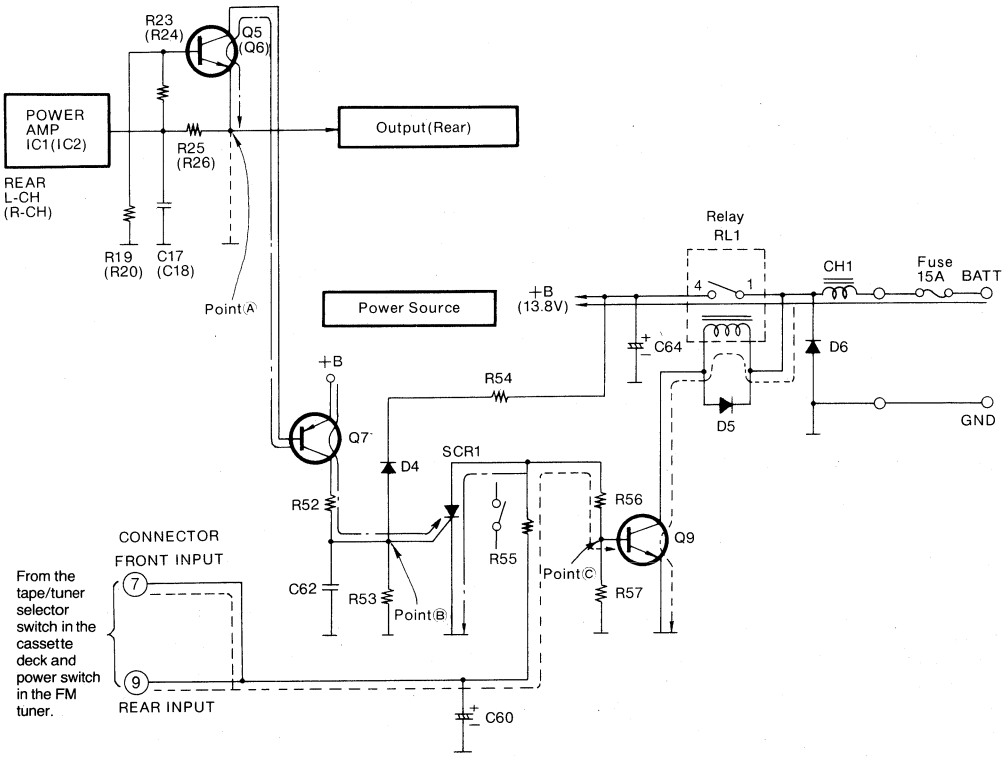


fig. 44

21. Dome Lamp

The Dome Lamp included in the RM-610, when properly wired to the vehicle, may be controlled in the following ways by switching.

(1) The lamps illuminate only when the doors are opened
(2) Only the lamp on the left side illuminates
(3) Only the lamp on the right side illuminates
(4) The lamps are off

Method of wiring to the vehicle

(1) For GM vehicles (with the door switch on the negative side of the battery)

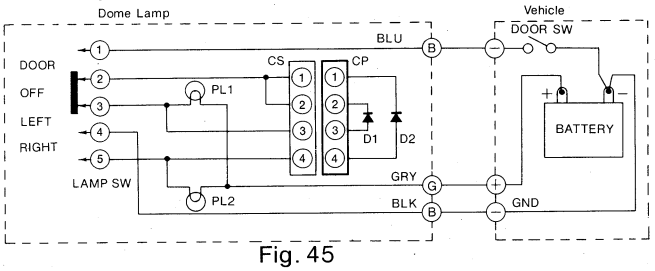


Fig. 45

Note: On some models, the positive line from the battery is not wired to the dome lamps. For these models, the positive line should be wired directly from the battery.

(2) For Ford vehicles (with the door switch on the positive side of the battery)

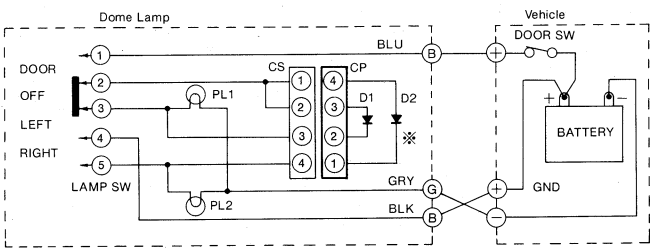


Fig. 46

Notes: ●On Ford vehicles, insert the diode plugs in the opposite direction (as indicated by the ※ mark in the above figure).

●On some models, the negative line from the battery is not wired to the dome lamps. For these models, the negative line should be wired directly from the battery.

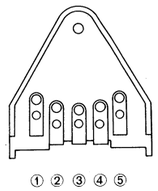


Fig. 47 LAMP SWITCH (TOP VIEW)

22. Basic Logic Circuit

The digital system is composed to need 4 modes; AND, OR, NOT and DELAY.
As the DELAY can be made by composing 3 modes, therefore, the digital system is enough 3 modes only; the AND, the OR and the NOT.

AND CIRCUIT

The AND circuit, called an AND gate, turns the output (X) to "1" when both inputs A and B are "1".
In the equivalent circuit, the AND circuit appears a signal "1" at the output (X), when the switches A and B is in the ON position, that is only at "1".
The truth table shows the output (X) logic condition against combination of the inputs A and B.
The AND circuit is logic-formularized as follows:

$X=A\cdot B$

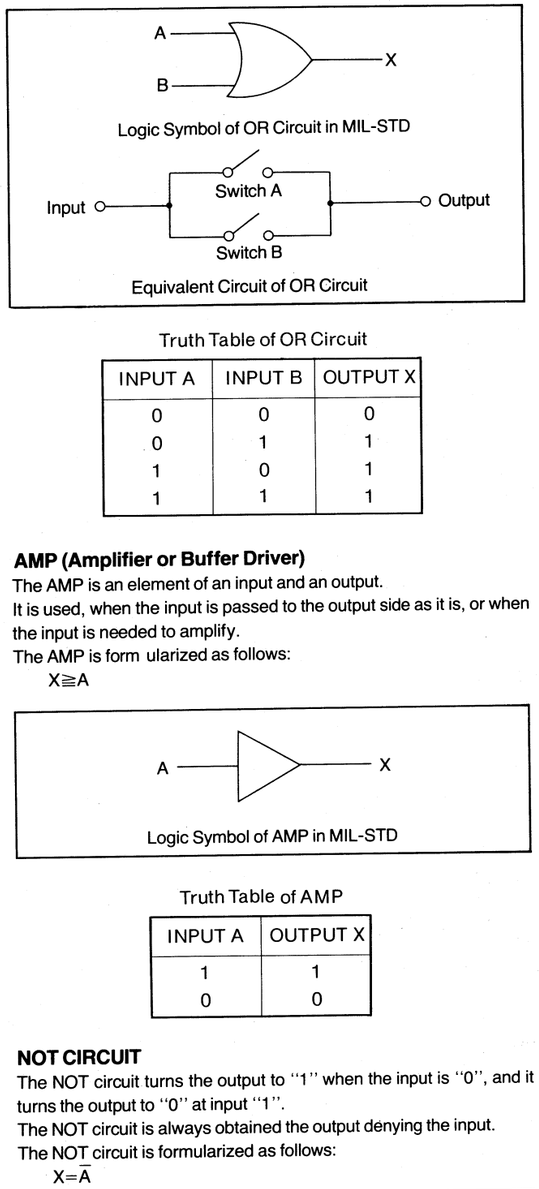
Truth Table of AND Circuit

INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	0
1	0	0
1	1	1

OR CIRCUIT

The OR circuit turns the output to "1", when either the input A or the B is "1", or when both the inputs A and B are "1".
In the circuitry, the OR circuit appears a signal "1" at the output (X), when either the switch A or the B is in the ON position, or when both the A and B is ON.
The OR circuit is formularized as follows:

$X=A+B$



Truth Table of OR Circuit

INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	1
1	0	1
1	1	1

AMP (Amplifier or Buffer Driver)

The AMP is an element of an input and an output.
It is used, when the input is passed to the output side as it is, or when the input is needed to amplify.
The AMP is form ularized as follows:

$X \geqq A$

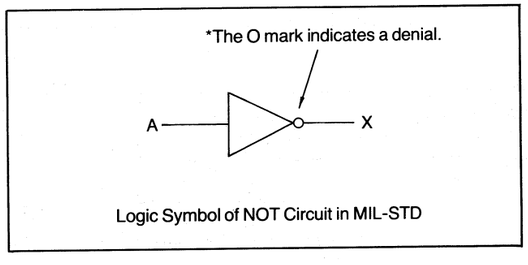
Truth Table of AMP

INPUT A	OUTPUT X
1	1
0	0

NOT CIRCUIT

The NOT circuit turns the output to "1" when the input is "0", and it turns the output to "0" at input "1".
The NOT circuit is always obtained the output denying the input.
The NOT circuit is formularized as follows:

$X=\overline{A}$



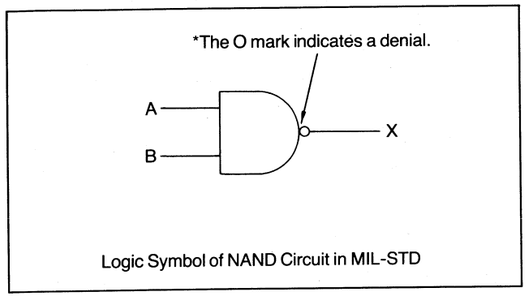
Truth Table of NOT Circuit

INPUT A	OUTPUT X
1	0
0	1

NAND CIRCUIT

The NAND circuit is the AND circuit connected with the NOT circuit, and it turns the output to "0", when all the inputs are "1".
The NAND circuit is formularized as follows:

$X=\overline{A\cdot B}$



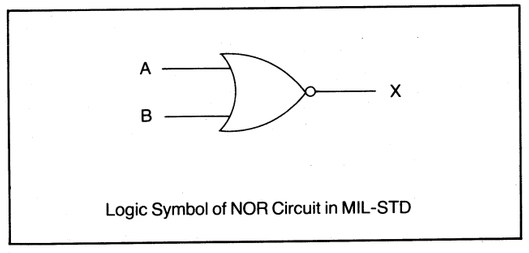
NAND Circuit

INPUT A	INPUT B	OUTPUT X
0	0	1
0	1	1
1	0	1
1	1	0

NOR CIRCUIT

The NOR circuit is the OR circuit connected with the NOT circuit, and it turns the output ot "1", when all the inputs are "0".
The NOR circuit is formularized as follows:

$X=\overline{A+B}$

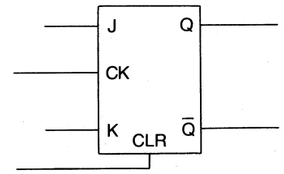


NOR Circuit

INPUT A	INPUT B	OUTPUT X
0	0	1
0	1	0
1	0	0
1	1	0

JK FLIP-FLOP:

The JK Flip-Flop is one of the most versitile types of binary storage elements in use.
A "Truth Table" is a chart of output conditions for a given set of input conditions. A truth table and logic symbol are shown in as below.

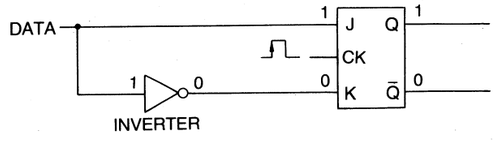


	INPUT				OUTPUT	
	CLR(CLEAR)	CK(CLOCK)	J	K	Q	Q
A	0	X	X	X	0	1
B	1	↑	0	0	Qo	$\overline{Qo}$
C	1	↑	1	0	1	0
D	1	↑	0	1	0	1
E	1	↑	1	1	TOGGLE	

INPUT/OUTPUT CONDITIONS (TRUTH TABLE)

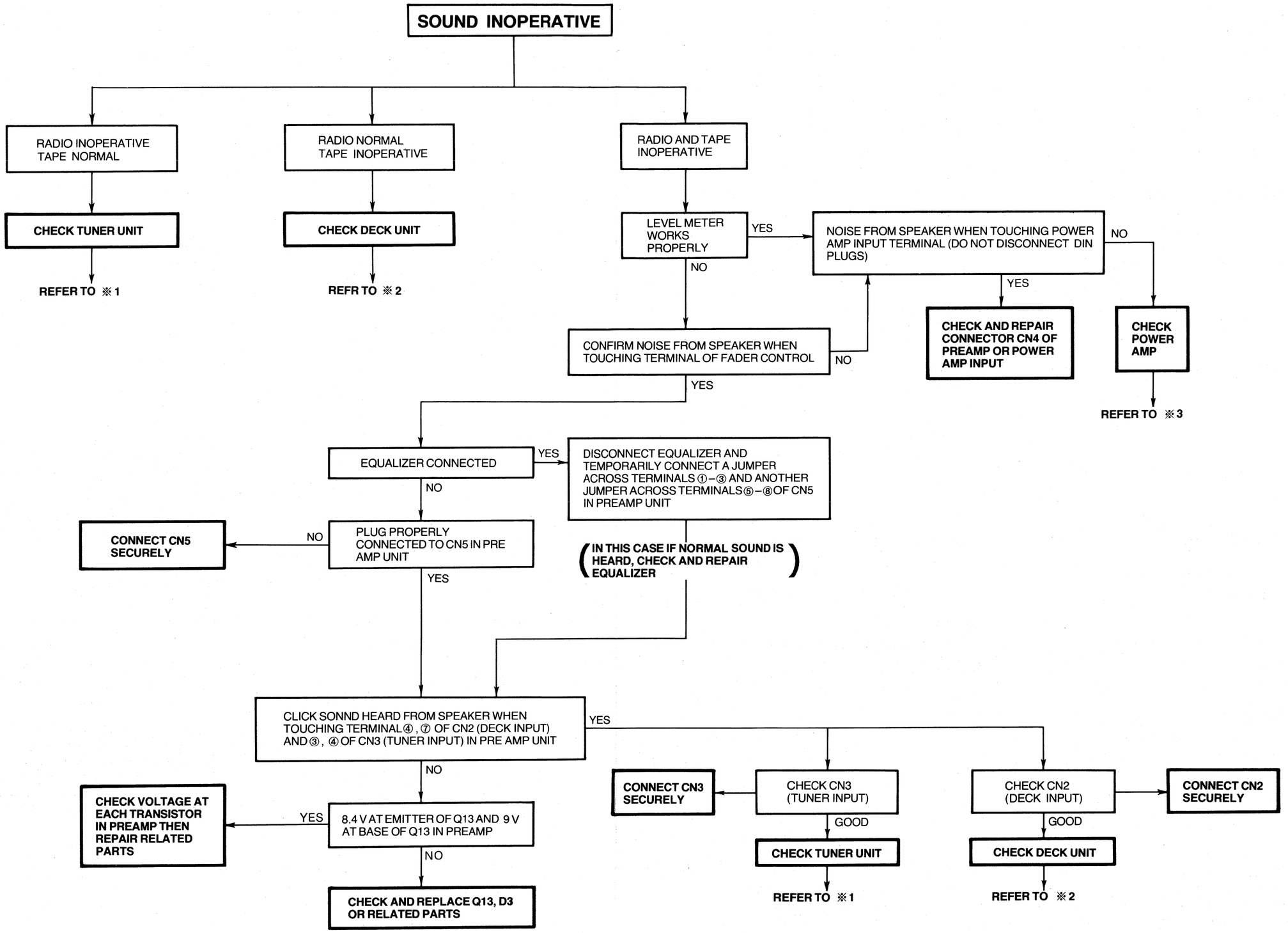
A) When a 0 (low level) is applied to the CLR input, the JK Flip-Flop is in the clear state. At this time the Q output will be 0 (low level) and the Q output will be 1 (high level). When the CLR. input is low, the CK, J and K input levels have no bearing on the output and are considered irrelevant (X).
B) In the following conditions, the CLR is 1 and the Flip-Flop is active. If the J & K inputs are at 0 and a clock transition is applied to CK, the Q and Q inputs will remain at their previous conditions (in memory).

C, D) Refer to following diagram.

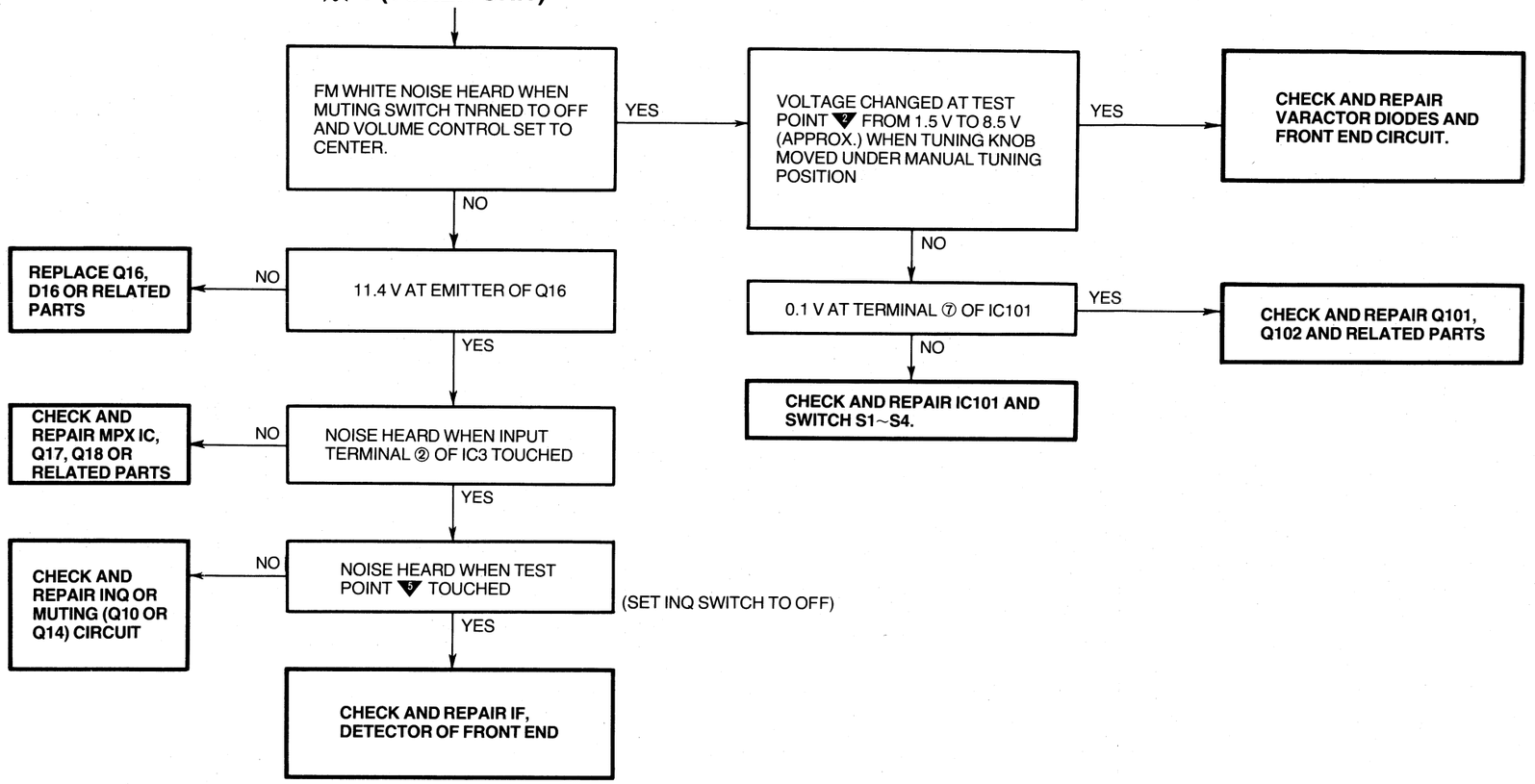


If data is applied to J and K, and a clock transition is presented to CK, the data is transferred to Q and Q. This information is stored in the Flip-Flop and the outputs remain the same even if data switches. The output is only effected by a clock pulse.
E) When J and K are high the Flip-Flop will toggle. In other words, the output will change to its compliment (1 to 0) with every clock transition.

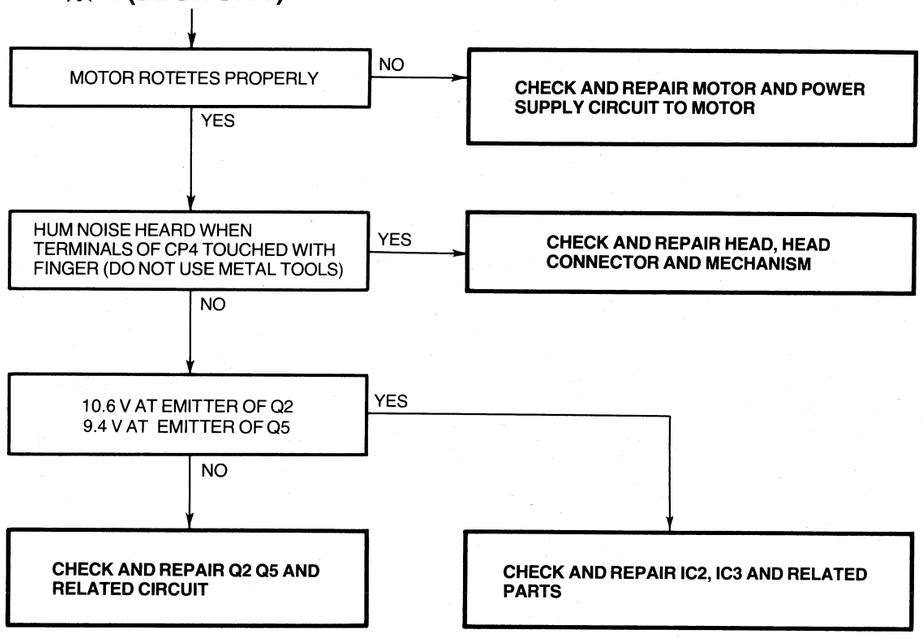
23. TROUBLESHOOTING GUIDE(Refer to Schematic Diagram for Details)



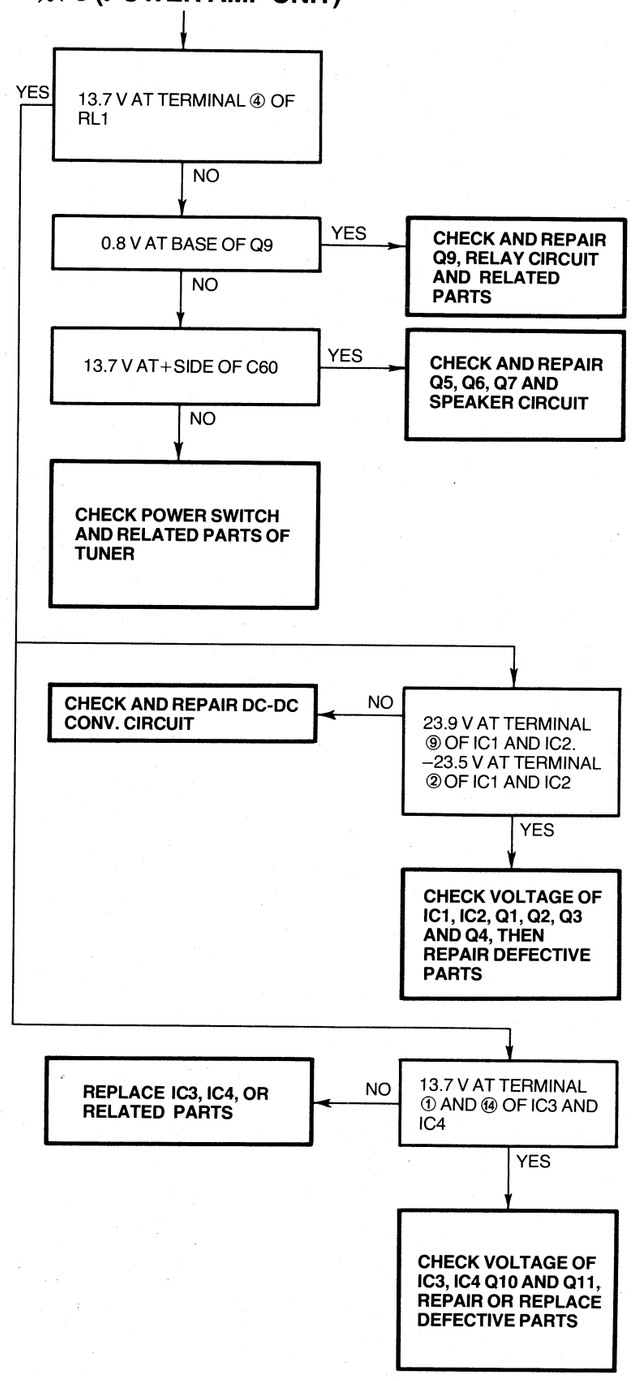
※ 1 (TUNER UNIT)



※ 2 (DECK UNIT)



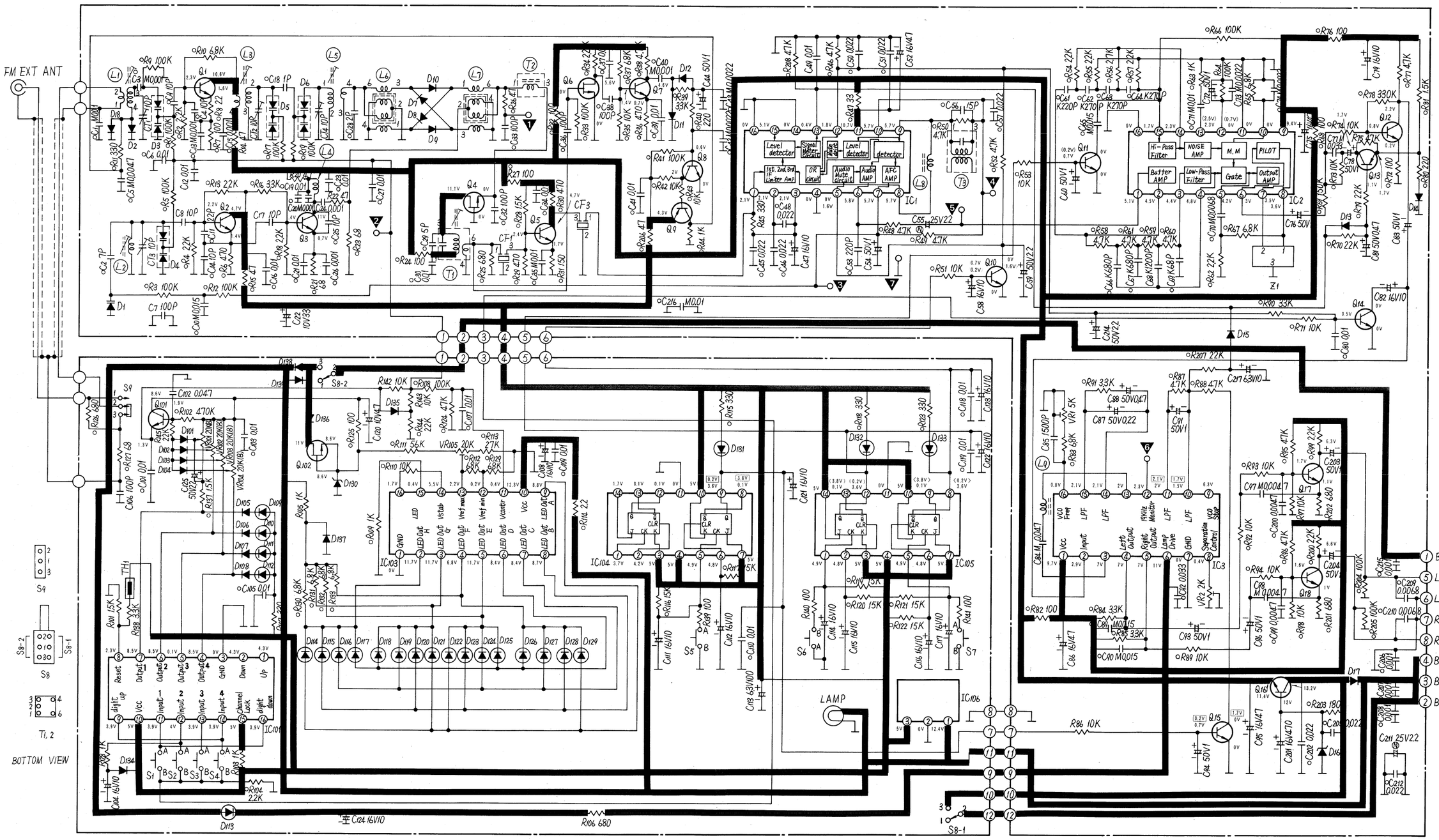
※ 3 (POWER AMP UNIT)



FM TUNER SCHEMATIC DIAGRAM-MODEL RM-610

Q1	D1	D2, 18	D3 ~ 6	Q2	Q3	D7 ~ 10	Q4	Q5	Q6	Q7	Q8	Q9	D11, 12	IC1
2SC2026	1S2687	MA56	RVD1SV55-03	2SC2671	2SC2671	RVD1SS97	2SK49	2SC2295	2SK49	2SC2295	2SD601	2SB709	1S2473	AN377SD
RF AMP	AFC	AGC	TUNING	OSC	BUFFER AMP	MIX	IF AMP	IF AMP	AGC AMP	AGC AMP	AGC AMP	AGC AMP	RECT	IF AMP & DET

Q10	D15	Q11	IC2	D13	Q12	Q13	Q14	D14
2SD601	MA150	2SD601	RVILA2101	0A90	2SD601	2SB709	2SD601	MA27B2
SWITCHING	SWITCHING	SWITCHING	I.N.Q	SWITCHING	AF AMP	SWITCHING	SWITCHING	AOC

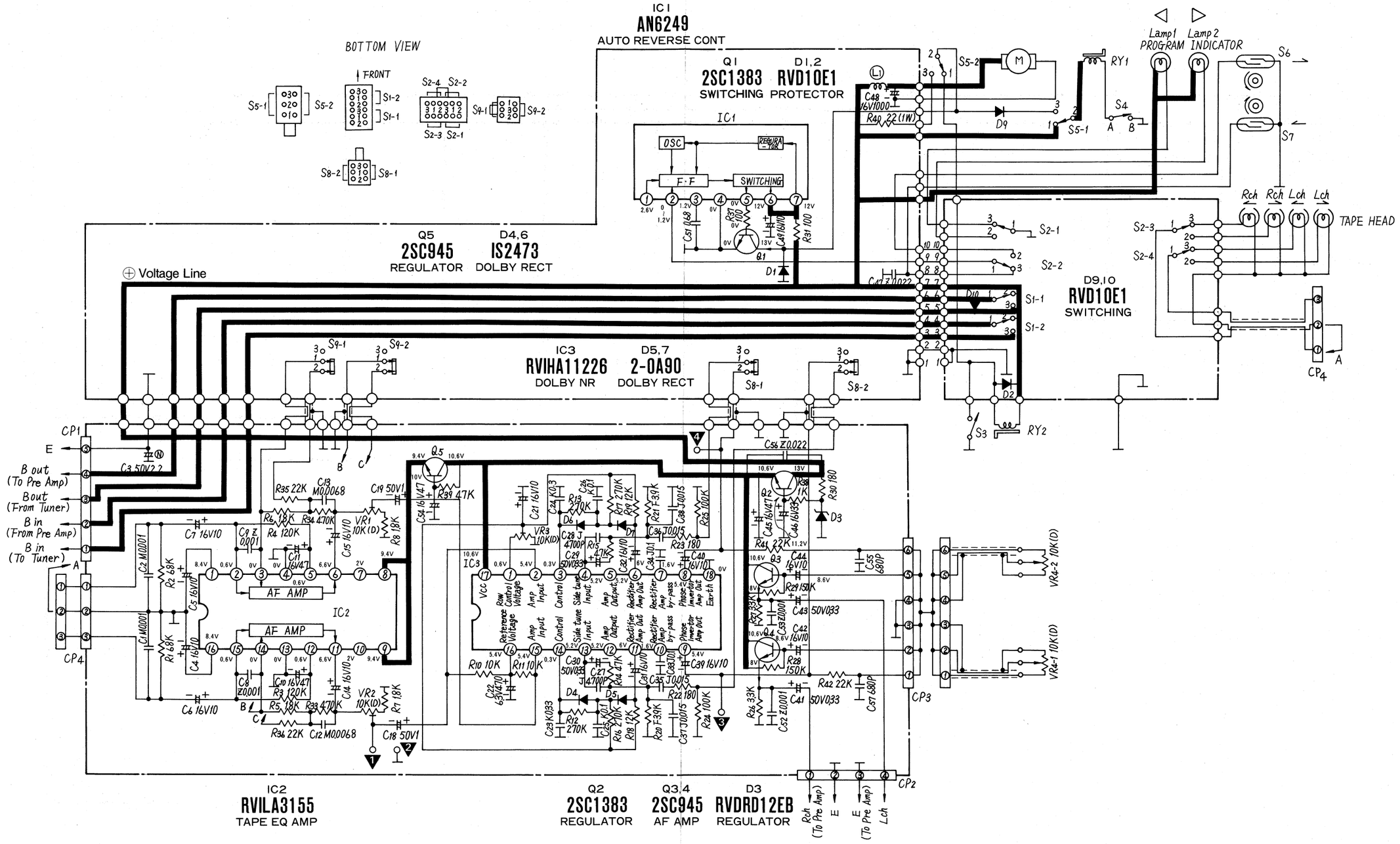


D137	D134, 139	Q101	D101~104	IC101	D105~108	D109~112	D113	D114~129	IC103	IC104, 105	D131	D132	D133	IC106
RVDRD12EB	1S2473	2SC1327	1S2473	RVIM51231P	1S2473	RVDSLS31URA	RVDSLS31URA	RVDSLS31GGMA	RVIUAA170	RVIDM7473N	RVDSLS31URA	RVDSLS31URA	RVDSLS31URA	RVIUPC14305
REGULATOR	SWITCHING	AOC	SWITCHING	CHANNEL SELECTER	SWITCHING	CHANNEL IND.	STEREO IND.	FREQ. IND.	FREQ. IND. CONTROL	SWITCHING	STEREO IND.	ANL IND.	SQUELCH IND.	REGULATOR

D130	Q102	D135	D136	D138
RVDMZ309-1A	2SK34	MA27B2	0A90	RVD10E1
REGULATOR	REGULATOR	REGULATOR	PROTECTOR	PROTECTOR

IC3	Q15	Q16	Q17, 18	D17	D16
RVILA3350	2SD601	2SC1847	2SD601	RVD10E1	RVDRD12EB
MPX	SWITCHING	REGULATOR	AF AMP	PROTECTOR	REGULATOR

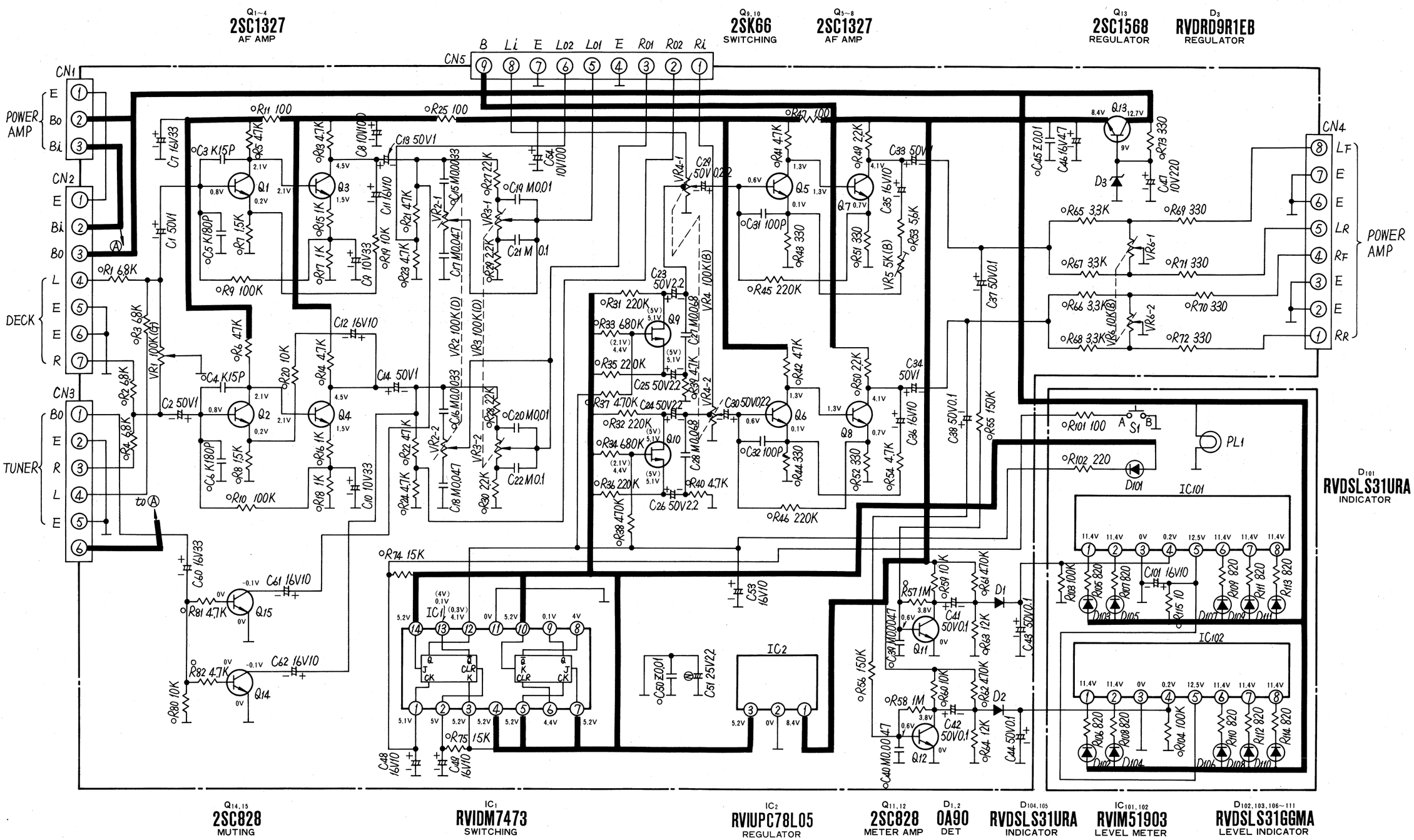
CASSETTE DECK SCHEMATIC DIAGRAM - MODEL RM-610



Notes:

1. S_{1-1}, S_{1-2}: Playback switch in "ON" position.
2. S_{2-1}~S_{2-4}: Auto reverse switch in "Forward" position.
3. S_3: Program switch.
4. S_4: Eject switch.
5. S_{5-1}, S_{5-2}: Playback/Fast forward, Rewind switch "playback" position.
6. $S_{6,7}$: Lead switch.
7. S_{8-1}, S_{8-2}: Dolby NR switch in "off" position.
8. S_{9-1}, S_{9-2}: Tape selector switch in "CrO_2" position.
9. DC voltage measurements are taken with VTVM with reference to ground.

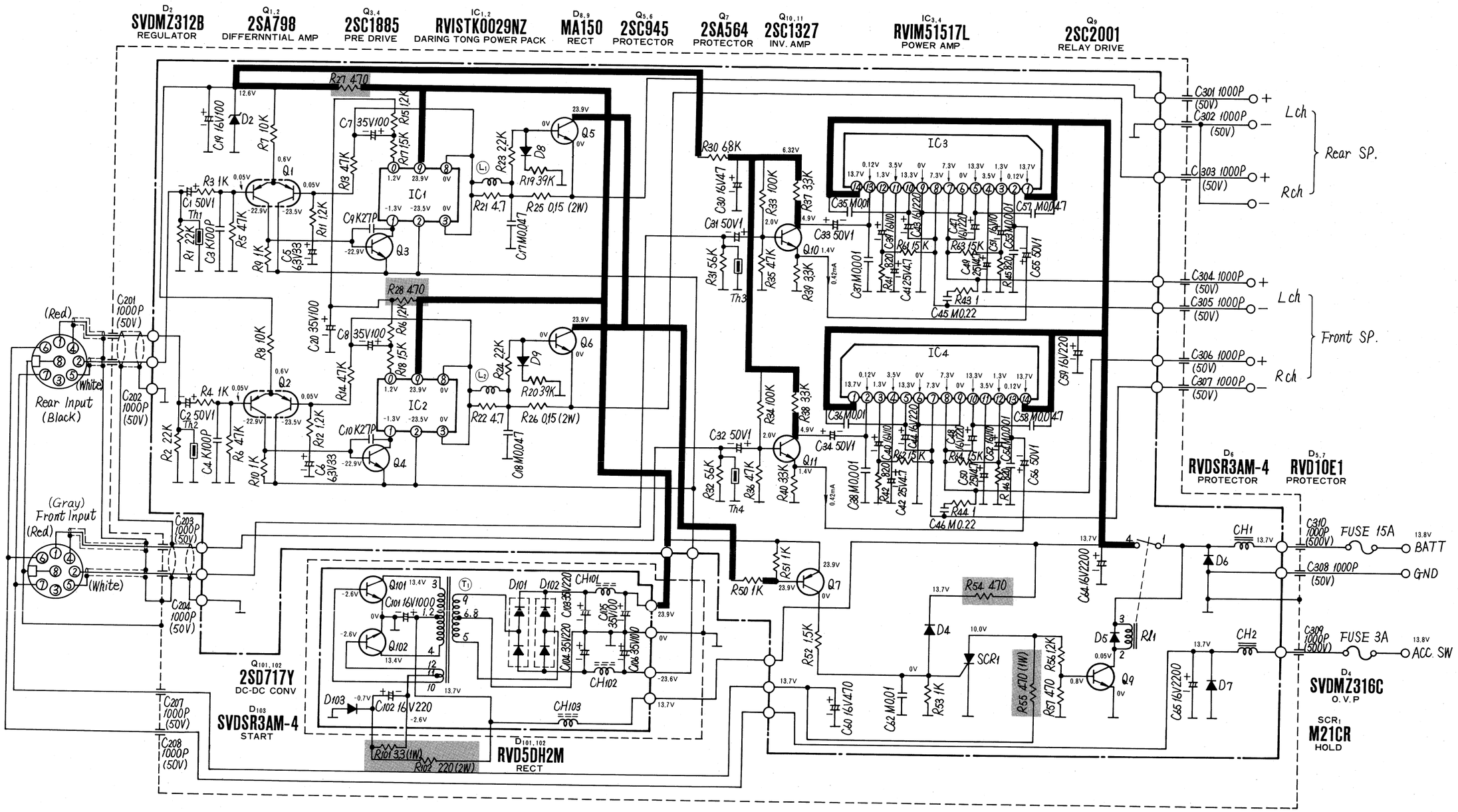
PREAMPLIFIER SCHEMATIC DIAGRAM -MODEL RM-610



Notes:

1. S_1: Loudness switch.
2. ○ mark...Chip resistors and capcaitors.
3. DC voltage measurements are taken with VTVM with reference to ground.
   ( )...Loudness switch in "ON" position.

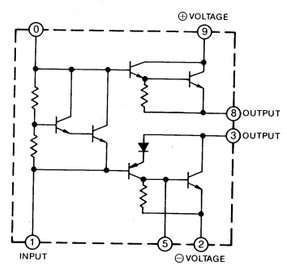
POWER AMPLIFIER SCHEMATIC DIAGRAM -MODEL RM-M610



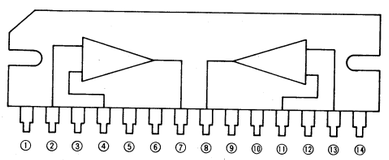
Note:

1. DC voltage measurements are taken with VTVM with reference to ground.

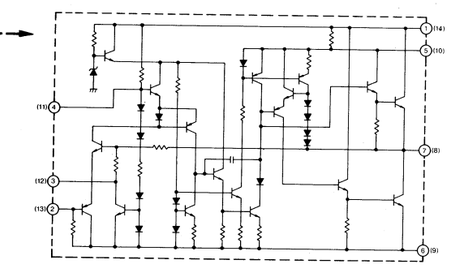
IC1,2



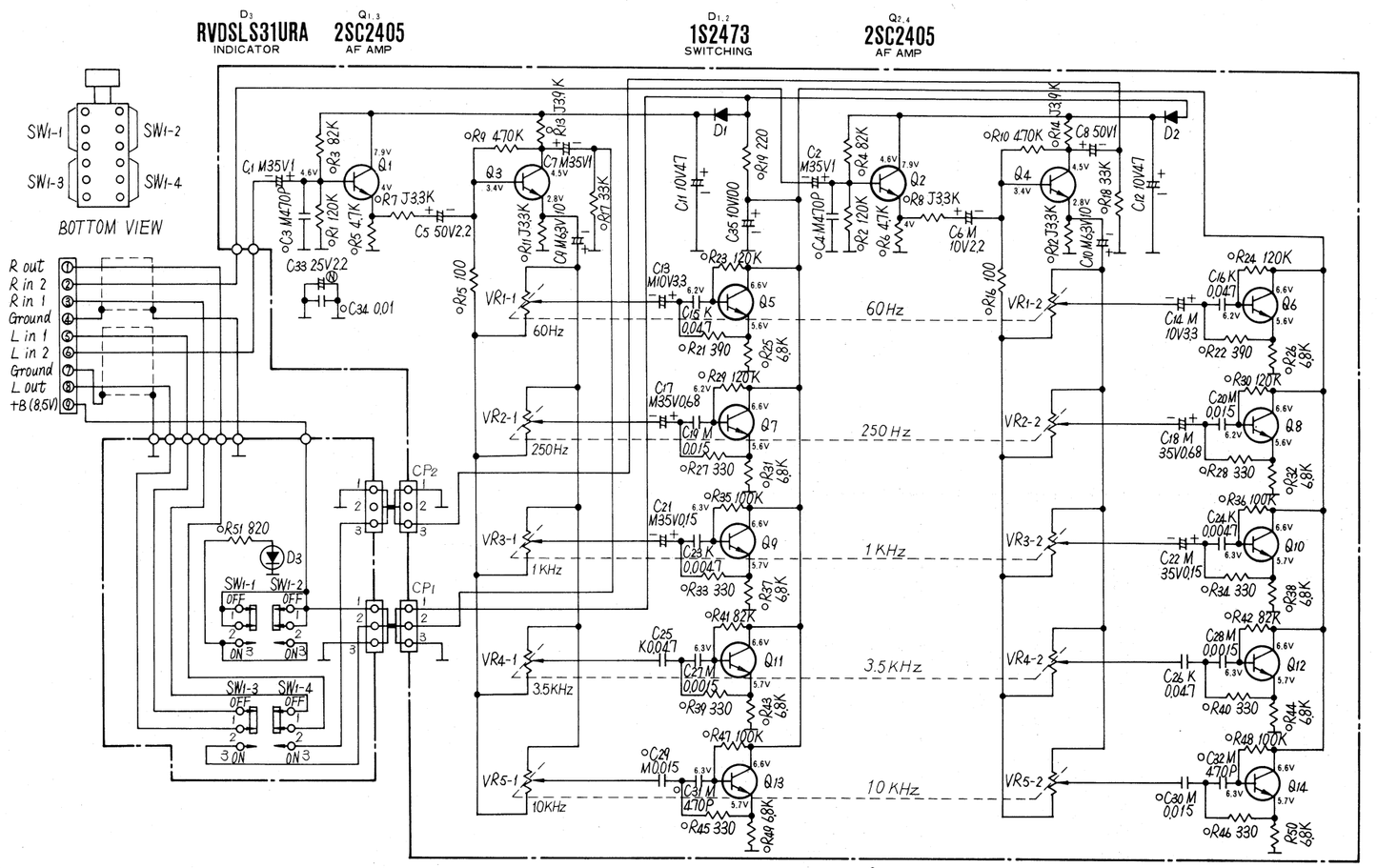
IC 3,4



① Supply voltage-L
② Input-L
③ Feedback-L
④ Ripple filter-L
⑤ Boot strap-L
⑥ Ground-L
⑦ Output-L
⑧ Output-R
⑨ Ground-R
⑩ Bootstrap-R
⑪ Ripple filter-R
⑫ Feedback-R
⑬ Input-R
⑭ Supply voltage-R



SCHEMATIC DIAGRAM – MODEL RM-E610



Notes:

1. S_{1-1}～S_{1-4}: Equalizer switch in "OFF" position.
2. ○ mark...Chip resistors and capacitors.
3. DC voltage measurements are taken with an electronic voltmeter with reference to ground.

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